TJ GREEN ASSOCIATES, LLC

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Virtual Training Course Outline

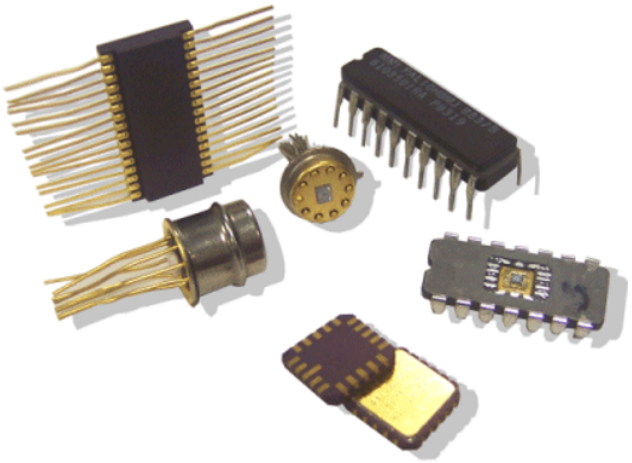
MIL-STD-883 TM 2010 Visual Inspection

(1 Session 3 hrs)

Instructor: Thomas Green, TJ GreenAssociates, LLC

INSPECT PER TM 2010

32 Pin CERDIP



This course is an addendum to the Pre Cap Visual MIL-STD-883 TM 2017 inspection class (4 sessions) and its best to take that class first before registering for this one. TM 2010 contains the full inspection criteria for Class S and B monolithic microcircuits. TM 2010 Microcircuit visual inspection is a flow down requirement from Mil-Prf-38535. The primary focus of this session will be on the “low mag” visual requirements for component attach and wire bond, which differ from the TM 2017 hybrid visual inspection criteria. TM 2010 also contains additional die attach and wire bond requirements not addressed in TM 2017. We will also briefly review the high mag inspection requirements for ICs and MMICs with a special emphasis on Class S products.

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Course Outline

- **Mil-Prf-38535 Integrated Circuit (Microcircuits) General Spec flow down requirements for visual inspection**

- **Low Mag Criteria (30-60X)**
  - Die Attach(eutectic and non-eutectic criteria)
  - Wirebond General (gold ball, wedge, and tailless)
  - Rebonding of monolithic devices.
  - Flip chip solder bump die (para 3.2.1.6)
  - Foreign material (para. 3.2.5)
  - Foreign Material Die Coated devices (para 3.2.5.1)

- **High Mag Criteria (special emphasis on Class S)**
  - Para 3.1.1-3.4 High Mag IC and MMIC Inspection
  - Para. 3.1.6. Film resistors
  - Para 3.1.7 Laser trimmed thin film resistors
  - Flip Chip Defects Scribe and Edge Cracks

- **Class Review with Q&A**

INSTRUCTOR BIO

Thomas J. Green has more than 43 years combined experience in industry/academia and the Department of Defense, including years developing curriculum and teaching industry professionals about microelectronics assembly-related packaging and processes. Serving as a Research Scientist at the U.S. Air Force Rome Air Development Center, Tom worked as a reliability engineer analyzing component failures from fielded avionic equipment. As a Senior Process Engineer with Lockheed Martin Astronautics in Denver, Tom was responsible for materials and processes used to assemble hybrid microelectronic components for military and aerospace applications. While with Lockheed, he gained invaluable experience in wirebond, die attach, thick- and thin-film substrate fabrication, hermetic sealing, and leak test processes. For the last 15 years, Tom's expertise has helped position his company as a recognized industry leader in teaching and consulting services for high-reliability military, space, and medical device applications. Tom is a Fellow of IMAPS (International Microelectronics and Packaging Society).