Course Notes

TJ GREEN ASSOCIATES, LLC

Pre Cap Visual Inspection

MIL-STD-883 TM 2017

Virtual Training
December 14-17, 2020

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Opening Remarks

- **Welcome**
- **Logistics**
- **Scope / Objectives**
- **Review Outline/TM 2017**

Course Goals and Objectives

- ➢ Know what to look for at Pre Cap visual inspection . . . what constitutes a “Reject”
- ➢ Learn how to navigate MIL-STD-883
- ➢ Understand TM 2017 and where and when to reference other Test methods outside of TM 2017
- ➢ Know what you are looking at and what constitutes a reject in the production flow along with the technical rationale to support the decision

Outline

SECTION 1: Introduction and Overview
  Mil Spec Visual Inspection Requirements Flowdown
  Component ID
  Foreign Material or F.O.D. inspection and source requirements

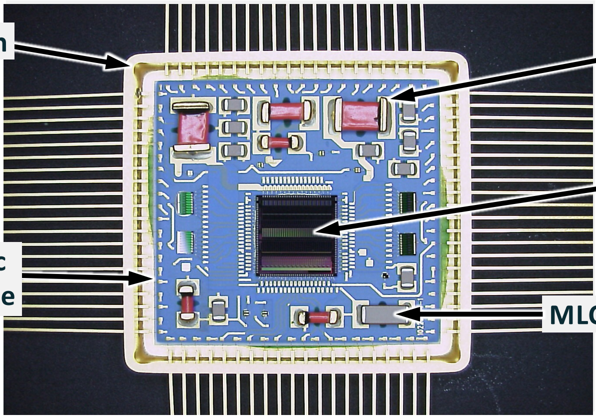
SECTION 2: Component Attach
  TM 2017 Low mag IC/MMIC die and substrate attach inspection criteria and non-planar capacitor/resistor criteria
  Solder Criteria

SECTION 3: Wire and Ribbon Bonding
  TM 2017 Low mag wire and ribbon bond inspection criteria

SECTION 4: High Mag IC Die and MMIC Inspection and Passives
  TM 2010 IC High Mag Inspection criteria
  MIL-STD-750 Die level Inspection Criteria TM 2017 Table 1
  TM 2032 Passive Component inspection criteria for substrates, capacitors, inductors and resistors

Course Notes

Hybrid Circuit (MIL-PRF-38534)



Kovar Can

Tantalum Capacitor

IC Chip

Ceramic Substrate

MLC Capacitor

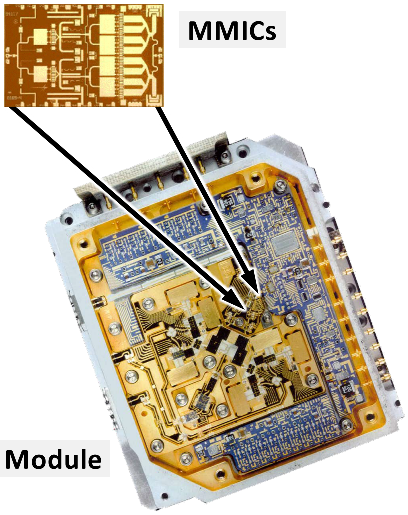
A Hybrid microcircuit contains two or more of a single type, or a combination of the following types of elements with at least one of the elements being active: Film microcircuit, Monolithic microcircuit, Semiconductor element, Passive chip or printed or deposited substrate elements.

MIL-PRF-38534

RF MMIC Microwave Modules (Monolithic Microwave Integrated Circuit)

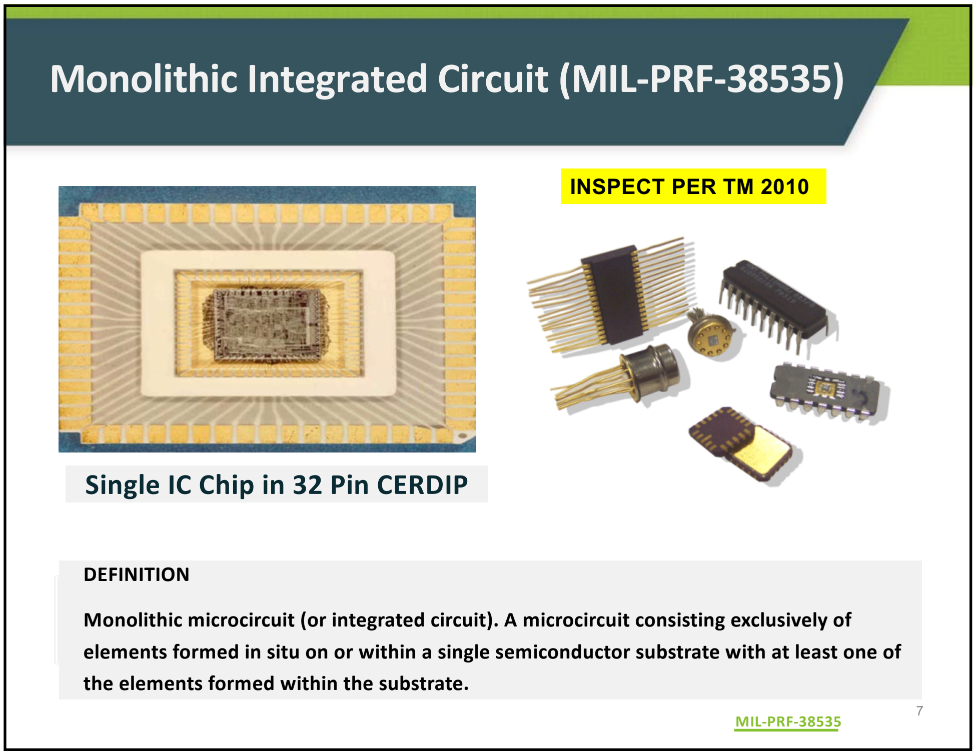
INSPECT PER MIL-STD 883 TM 2017

RF MMICs modules are also known as microwave hybrids or "MIC" hybrids and are similar to conventional Hybrids in many ways, but operate at much higher frequencies and make use of gallium arsenide (GaAs) and gallium Nitride (GaN) technology.



MMICs

RF MMIC Module



Monolithic Integrated Circuit (MIL-PRF-38535)

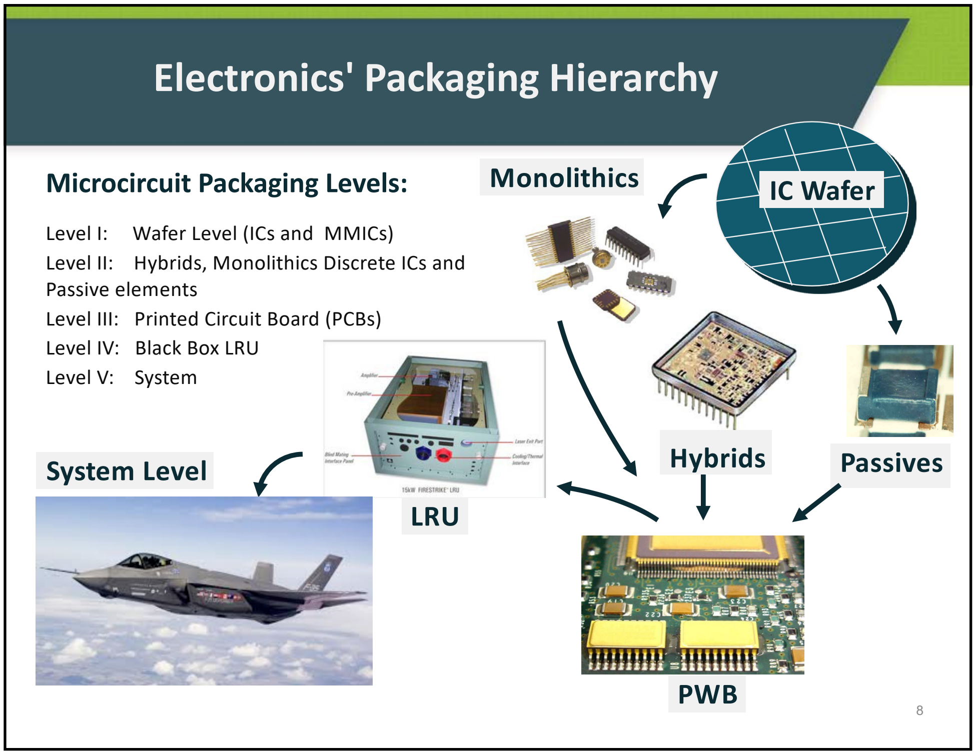
INSPECT PER TM 2010

Single IC Chip in 32 Pin CERDIP

DEFINITION

Monolithic microcircuit (or integrated circuit). A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate.

MIL-PRF-38535



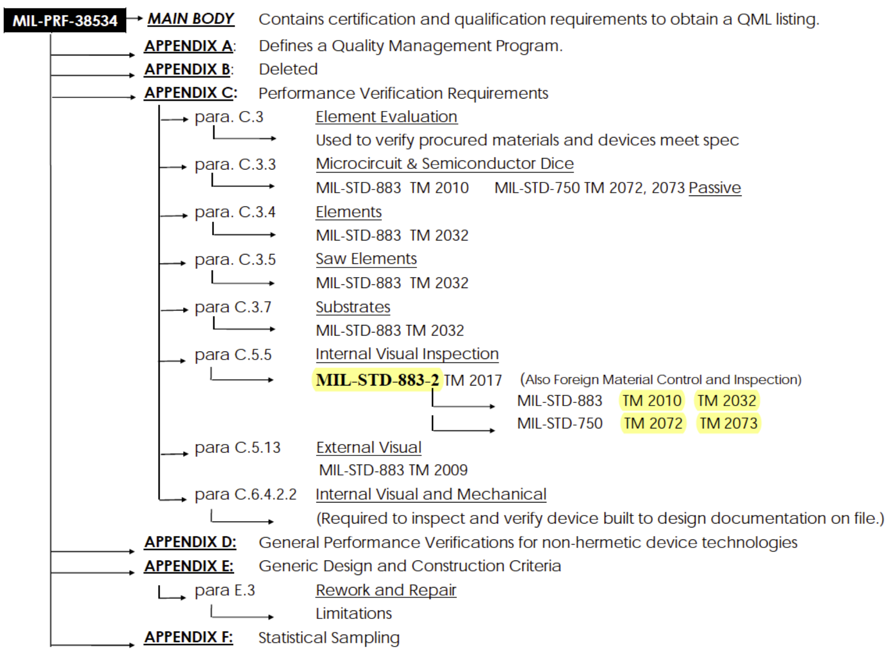
Electronics' Packaging Hierarchy

Microcircuit Packaging Levels:

Level I: Wafer Level (ICs and MMICs)
Level II: Hybrids, Monolithics Discrete ICs and Passive elements
Level III: Printed Circuit Board (PCBs)
Level IV: Black Box LRU
Level V: System

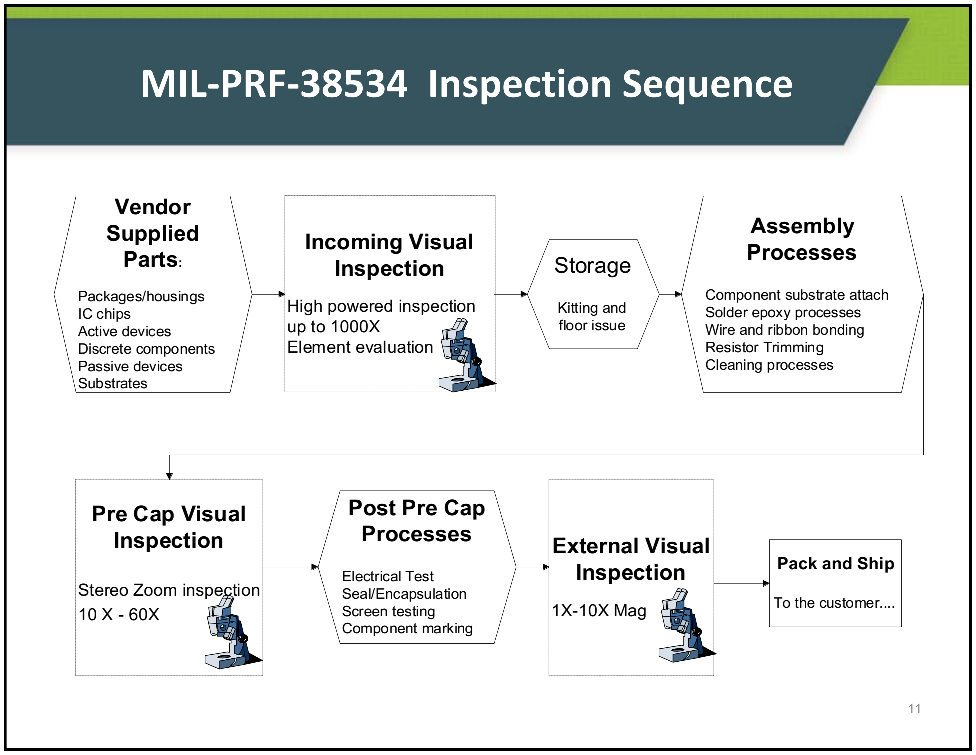
MIL-PRF-38534 (Hybrid Specification)

- A performance specification for Hybrid Microcircuits
- Defines a system and a process to verify device performance requirements (Main Body)
- Verification is accomplished through one of two Quality Management Programs (Appendix A)
- The main body describes the performance requirements and procedures on how to obtain a QML Listing
- 38534 is the governing document with frequent call outs to Test Methods defined in MIL-STD-883, including the visual inspection requirements in TM 2017 for Hybrids
- Its cousin is MIL-PRF-38535 Monolithic Devices



MIL-PRF-38534

- ***MAIN BODY*** Contains certification and qualification requirements to obtain a QML listing.
- **APPENDIX A**: Defines a Quality Management Program.
- **APPENDIX B**: Deleted
- **APPENDIX C**: Performance Verification Requirements
  - para. C.3 Element Evaluation
    - Used to verify procured materials and devices meet spec
  - para. C.3.3 Microcircuit & Semiconductor Dice
    - MIL-STD-883 TM 2010 MIL-STD-750 TM 2072, 2073 Passive
  - para. C.3.4 Elements
    - MIL-STD-883 TM 2032
  - para. C.3.5 Saw Elements
    - MIL-STD-883 TM 2032
  - para C.3.7 Substrates
    - MIL-STD-883 TM 2032
  - para C.5.5 Internal Visual Inspection
    - **MIL-STD-883-2** TM 2017 (Also Foreign Material Control and Inspection)
      - MIL-STD-883 TM 2010 TM 2032
      - MIL-STD-750 TM 2072 TM 2073
  - para C.5.13 External Visual
    - MIL-STD-883 TM 2009
  - para C.6.4.2.2 Internal Visual and Mechanical
    - (Required to inspect and verify device built to design documentation on file.)
- **APPENDIX D:** General Performance Verifications for non-hermetic device technologies
- **APPENDIX E:** Generic Design and Construction Criteria
  - para E.3 Rework and Repair
    - Limitations
- **APPENDIX F:** Statistical Sampling



MIL-PRF-38534 Inspection Sequence

Vendor Supplied Parts:
Packages/housings
IC chips
Active devices
Discrete components
Passive devices
Substrates

Incoming Visual Inspection
High powered inspection up to 1000X
Element evaluation

Storage
Kitting and floor issue

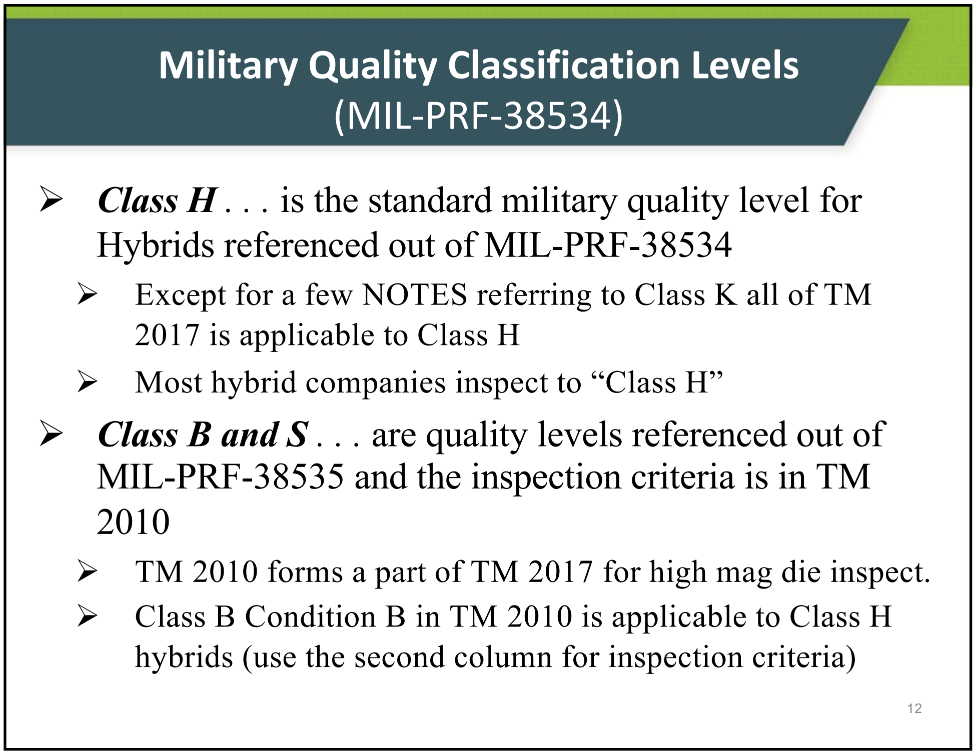
Assembly Processes
Component substrate attach
Solder epoxy processes
Wire and ribbon bonding
Resistor Trimming
Cleaning processes

Pre Cap Visual Inspection
Stereo Zoom inspection
10 X - 60X

Post Pre Cap Processes
Electrical Test
Seal/Encapsulation
Screen testing
Component marking

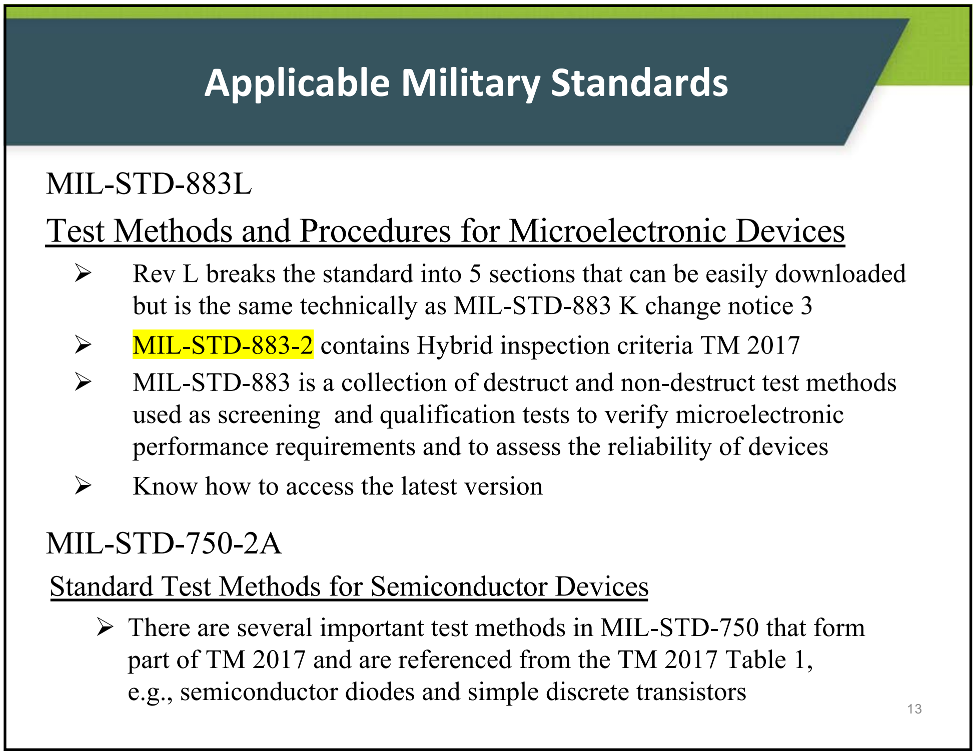
External Visual Inspection
1X-10X Mag

Pack and Ship
To the customer....



Military Quality Classification Levels (MIL-PRF-38534)

- ***Class H*** . . . is the standard military quality level for Hybrids referenced out of MIL-PRF-38534
  - Except for a few NOTES referring to Class K all of TM 2017 is applicable to Class H
  - Most hybrid companies inspect to “Class H”
- ***Class B and S*** . . . are quality levels referenced out of MIL-PRF-38535 and the inspection criteria is in TM 2010
  - TM 2010 forms a part of TM 2017 for high mag die inspect.
  - Class B Condition B in TM 2010 is applicable to Class H hybrids (use the second column for inspection criteria)



Applicable Military Standards

MIL-STD-883L

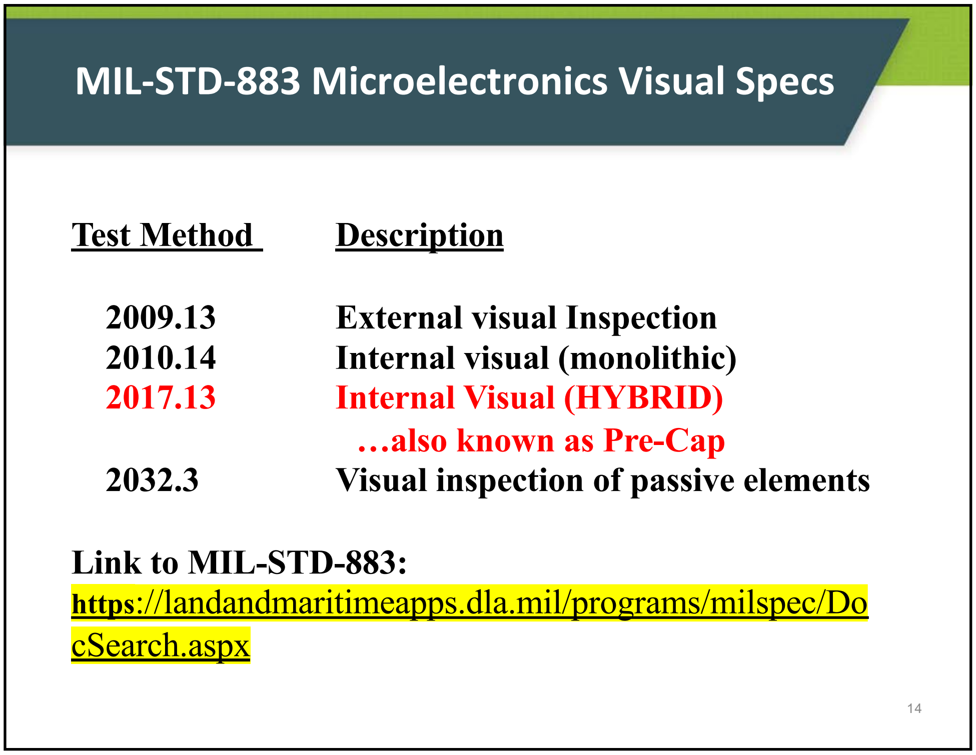
Test Methods and Procedures for Microelectronic Devices

- Rev L breaks the standard into 5 sections that can be easily downloaded but is the same technically as MIL-STD-883 K change notice 3
- MIL-STD-883-2 contains Hybrid inspection criteria TM 2017
- MIL-STD-883 is a collection of destruct and non-destruct test methods used as screening and qualification tests to verify microelectronic performance requirements and to assess the reliability of devices
- Know how to access the latest version

MIL-STD-750-2A

Standard Test Methods for Semiconductor Devices

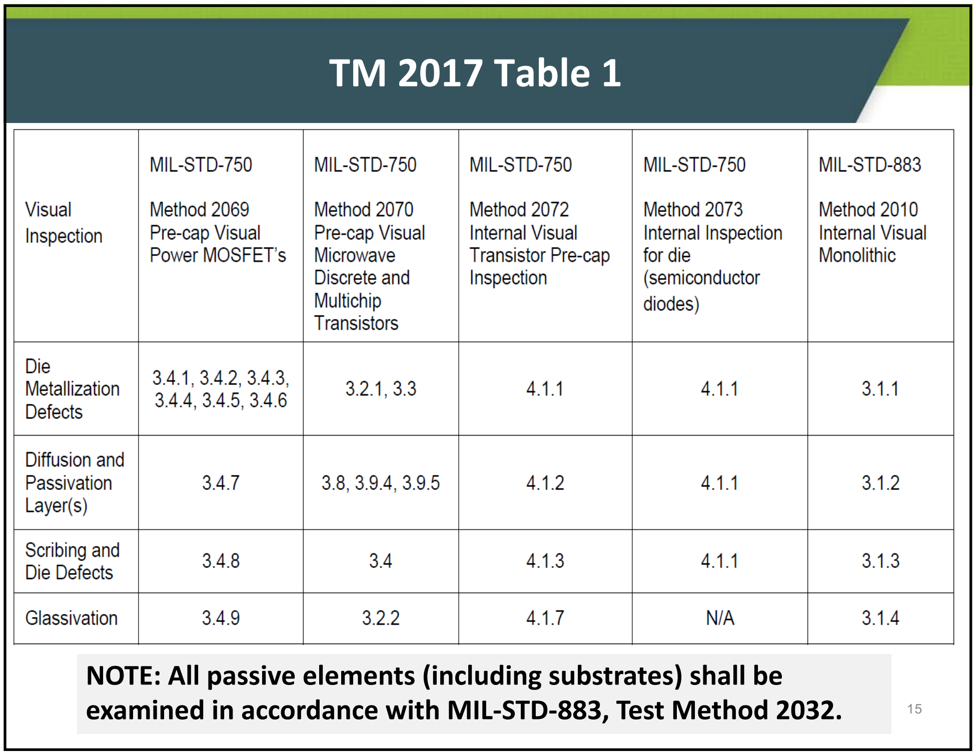
- There are several important test methods in MIL-STD-750 that form part of TM 2017 and are referenced from the TM 2017 Table 1, e.g., semiconductor diodes and simple discrete transistors



MIL-STD-883 Microelectronics Visual Specs

Test Method	**Description**
2009.13	**External visual Inspection**
2010.14	**Internal visual (monolithic)**
2017.13	**Internal Visual (HYBRID)** **…also known as Pre-Cap**
2032.3	**Visual inspection of passive elements**

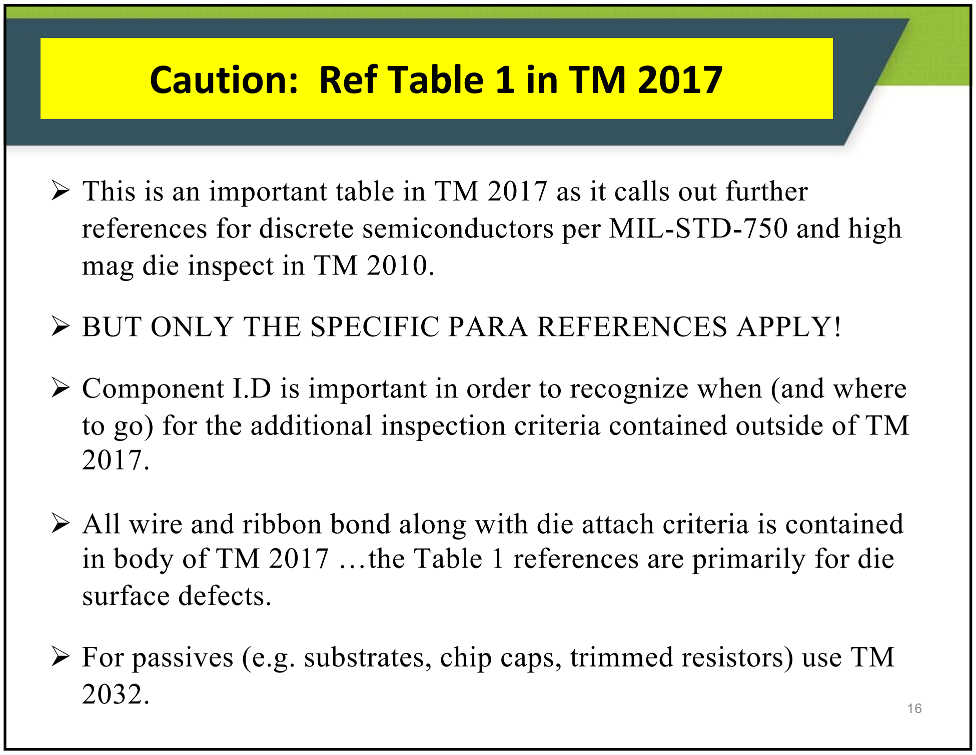
Link to MIL-STD-883:
https://landandmaritimeapps.dla.mil/programs/milspec/DocSearch.aspx



TM 2017 Table 1

Visual Inspection	MIL-STD-750 Method 2069 Pre-cap Visual Power MOSFET's	MIL-STD-750 Method 2070 Pre-cap Visual Microwave Discrete and Multichip Transistors	MIL-STD-750 Method 2072 Internal Visual Transistor Pre-cap Inspection	MIL-STD-750 Method 2073 Internal Inspection for die (semiconductor diodes)	MIL-STD-883 Method 2010 Internal Visual Monolithic
Die Metallization Defects	3.4.1, 3.4.2, 3.4.3, 3.4.4, 3.4.5, 3.4.6	3.2.1, 3.3	4.1.1	4.1.1	3.1.1
Diffusion and Passivation Layer(s)	3.4.7	3.8, 3.9.4, 3.9.5	4.1.2	4.1.1	3.1.2
Scribing and Die Defects	3.4.8	3.4	4.1.3	4.1.1	3.1.3
Glassivation	3.4.9	3.2.2	4.1.7	N/A	3.1.4

NOTE: All passive elements (including substrates) shall be examined in accordance with MIL-STD-883, Test Method 2032.



Caution: Ref Table 1 in TM 2017

- This is an important table in TM 2017 as it calls out further references for discrete semiconductors per MIL-STD-750 and high mag die inspect in TM 2010.
- BUT ONLY THE SPECIFIC PARA REFERENCES APPLY!
- Component I.D is important in order to recognize when (and where to go) for the additional inspection criteria contained outside of TM 2017.
- All wire and ribbon bond along with die attach criteria is contained in body of TM 2017 …the Table 1 references are primarily for die surface defects.
- For passives (e.g. substrates, chip caps, trimmed resistors) use TM 2032.

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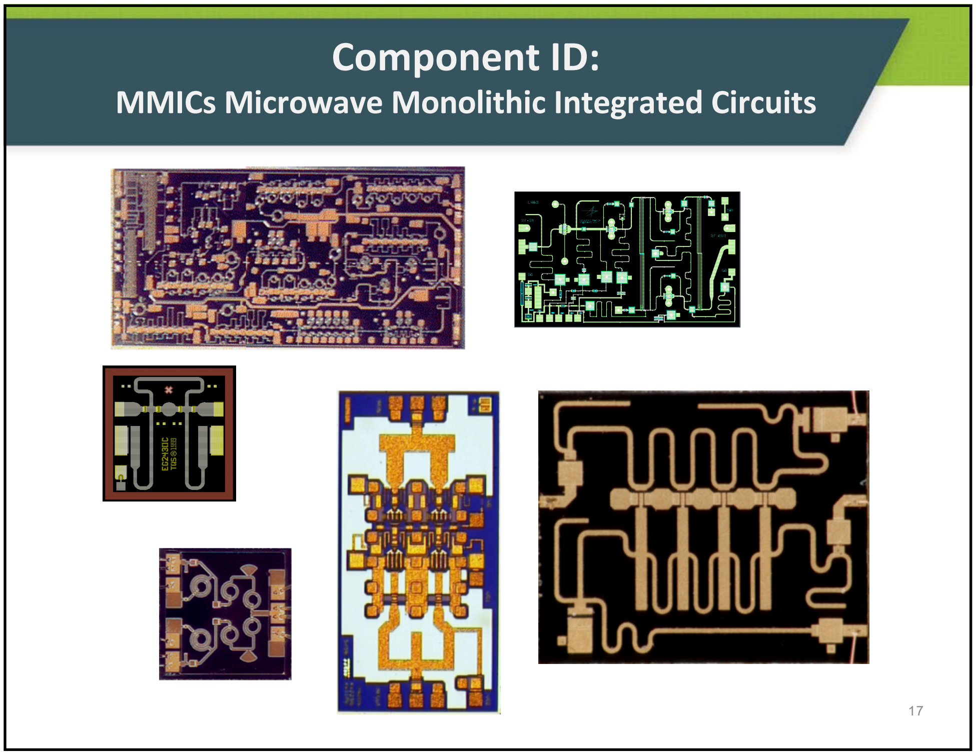
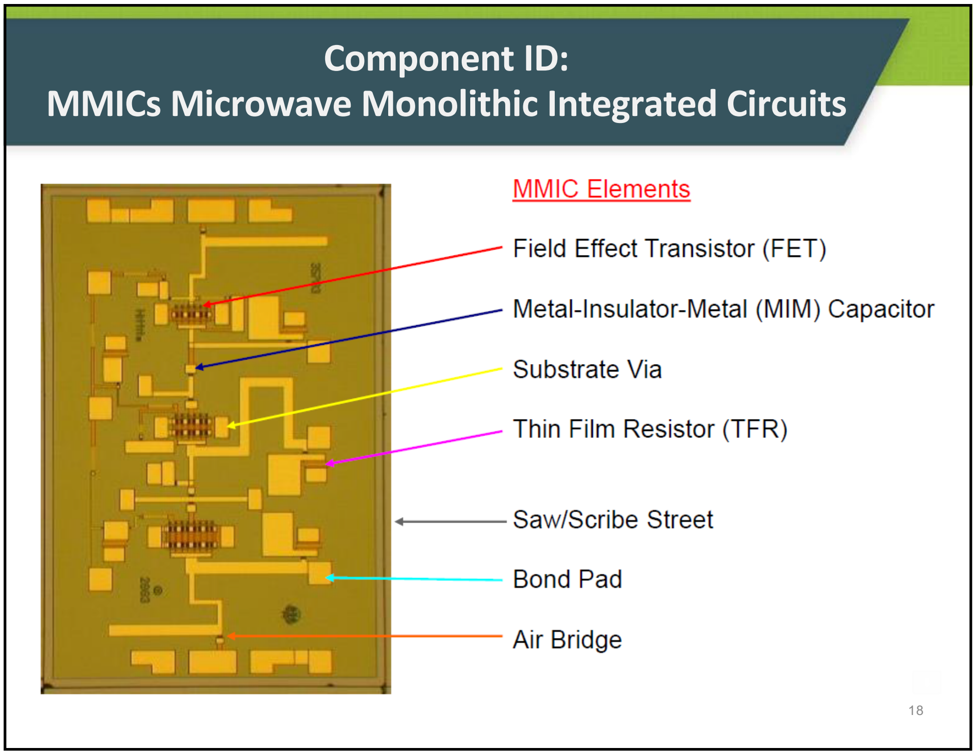


Component ID:
MMICs Microwave Monolithic Integrated Circuits

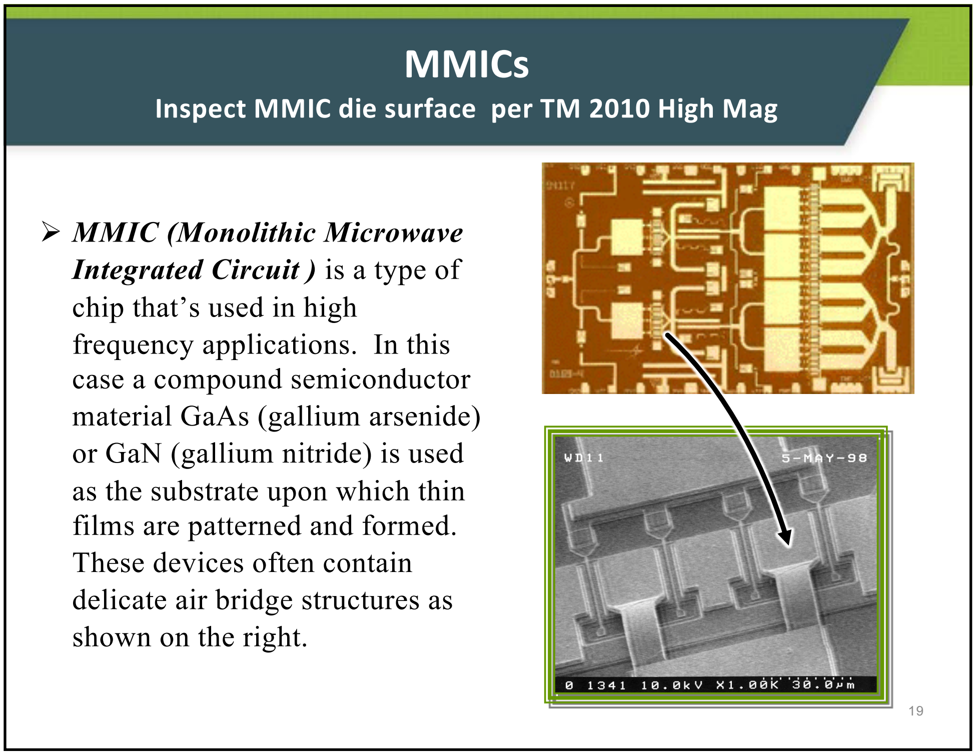


Component ID:
MMICs Microwave Monolithic Integrated Circuits

MMIC Elements

- Field Effect Transistor (FET)
- Metal-Insulator-Metal (MIM) Capacitor
- Substrate Via
- Thin Film Resistor (TFR)
- Saw/Scribe Street
- Bond Pad
- Air Bridge

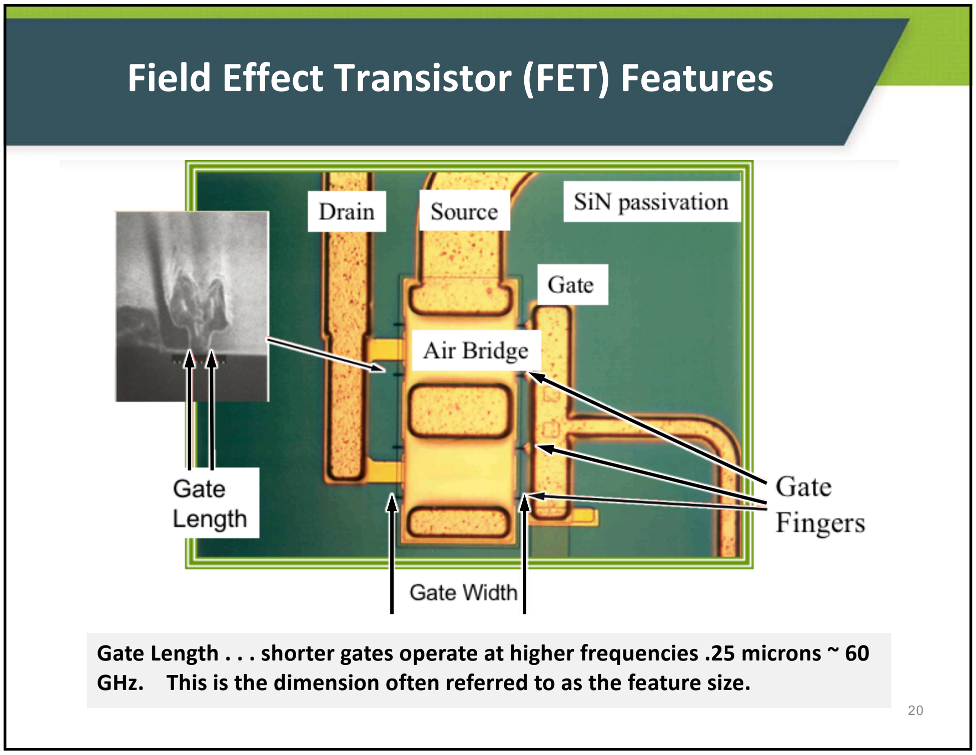
Course Notes



MMICs

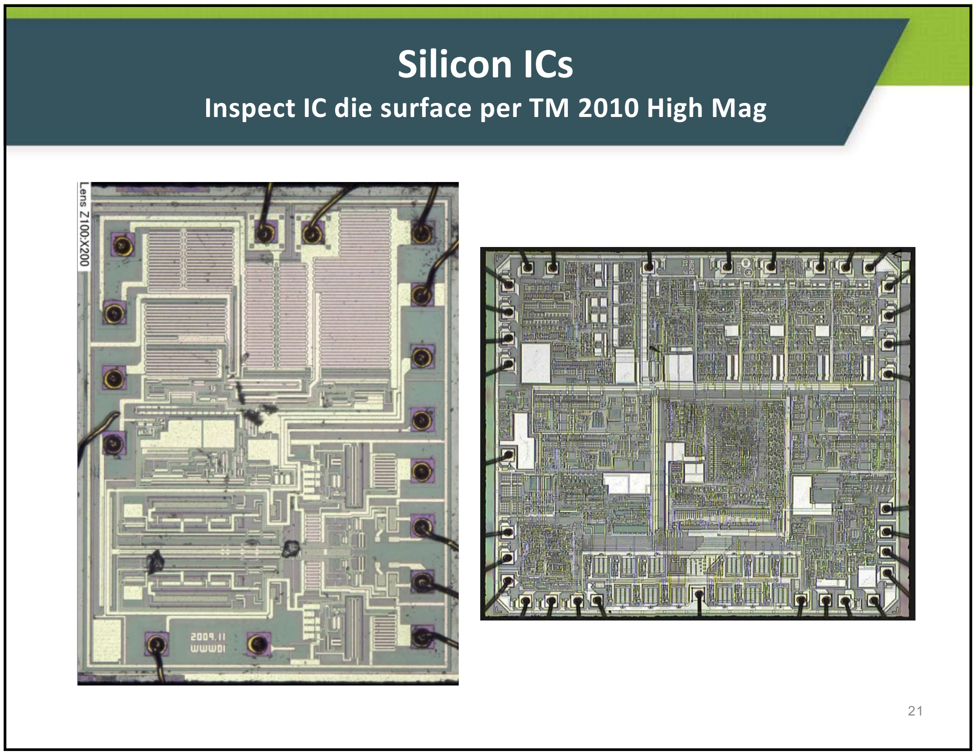
Inspect MMIC die surface per TM 2010 High Mag

- ***MMIC (Monolithic Microwave Integrated Circuit)*** is a type of chip that's used in high frequency applications. In this case a compound semiconductor material GaAs (gallium arsenide) or GaN (gallium nitride) is used as the substrate upon which thin films are patterned and formed. These devices often contain delicate air bridge structures as shown on the right.



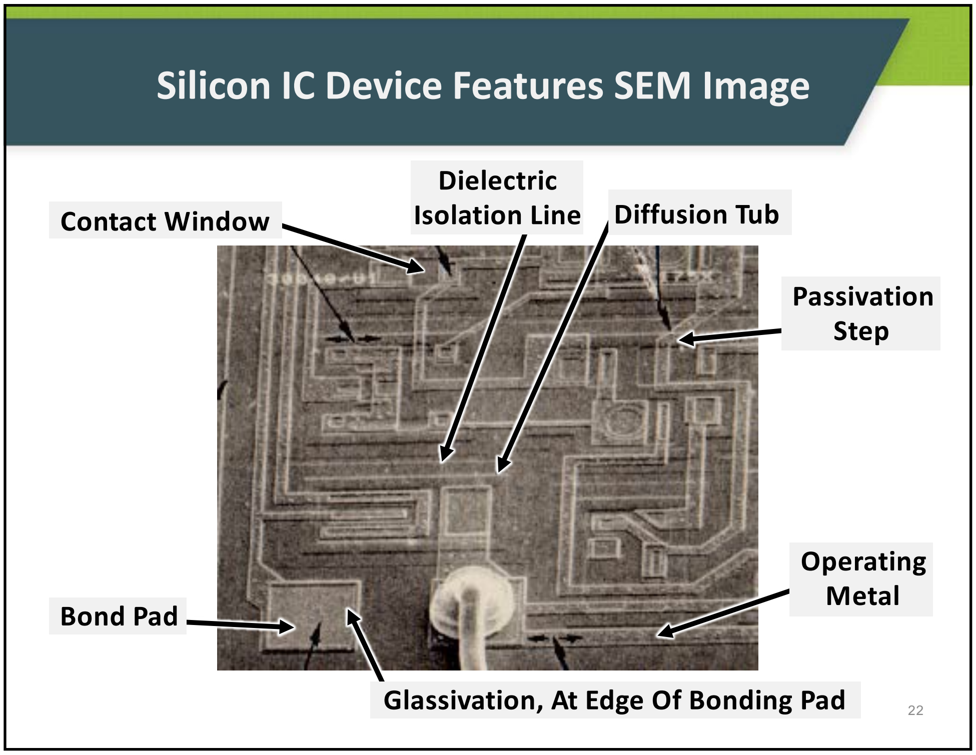
Field Effect Transistor (FET) Features

Gate Length . . . shorter gates operate at higher frequencies .25 microns ~ 60 GHz. This is the dimension often referred to as the feature size.



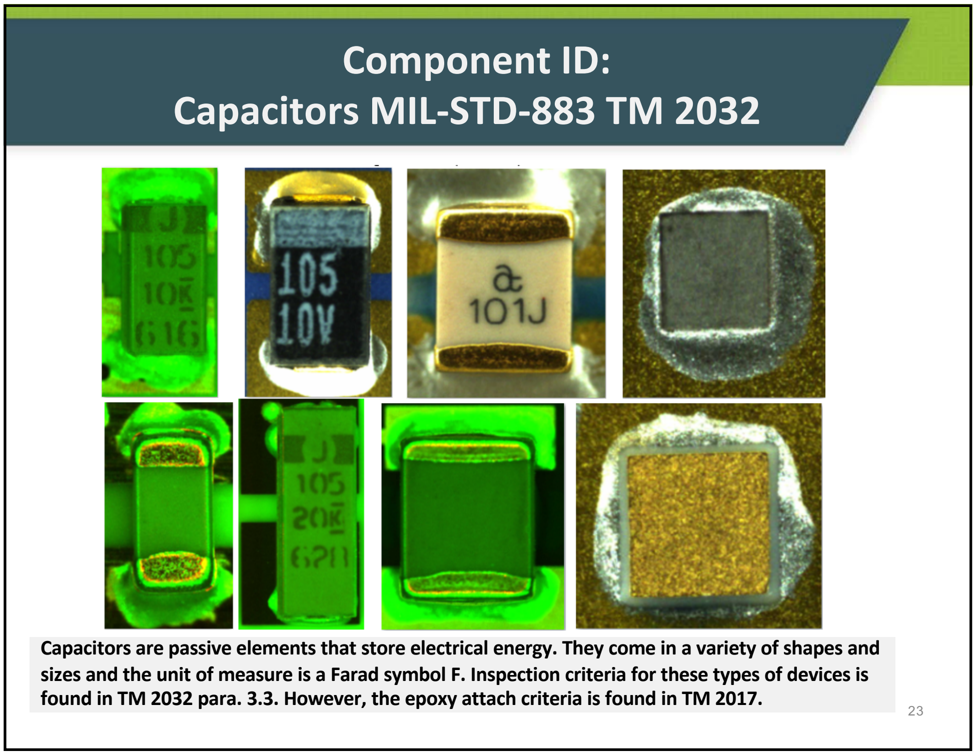
Silicon ICs

Inspect IC die surface per TM 2010 High Mag



Silicon IC Device Features SEM Image

Course Notes



Component ID: Capacitors MIL-STD-883 TM 2032

Capacitors are passive elements that store electrical energy. They come in a variety of shapes and sizes and the unit of measure is a Farad symbol F. Inspection criteria for these types of devices is found in TM 2032 para. 3.3. However, the epoxy attach criteria is found in TM 2017.

Component ID: Resistors MIL-STD-883 TM 2032

Laser trimmed thick film resistor

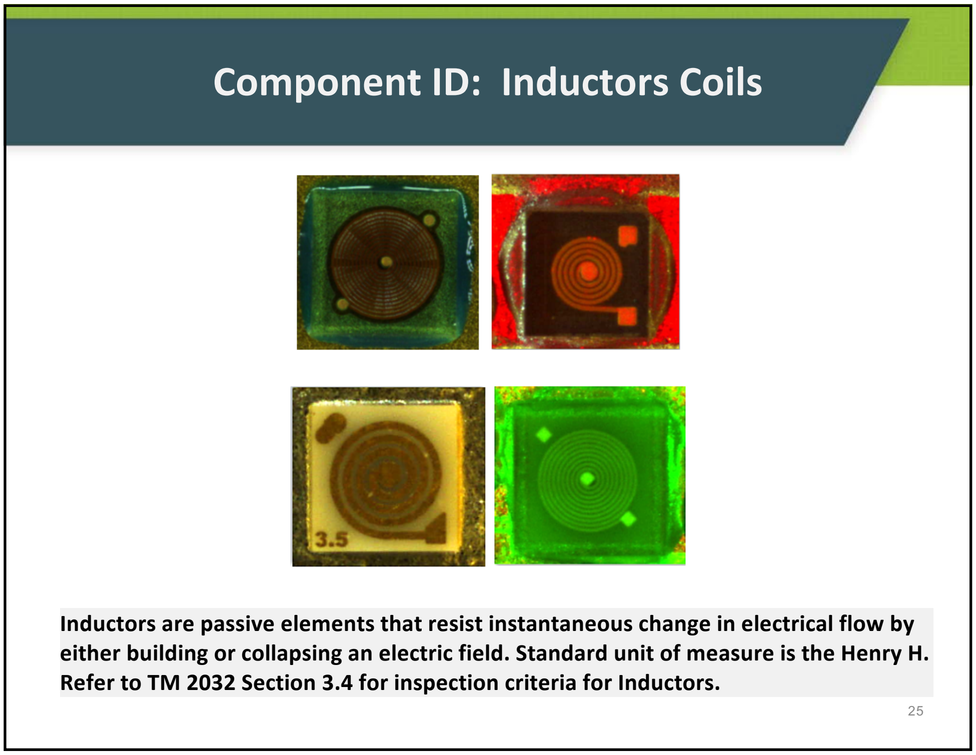
Multi Tap Thin film resistor

Select in test Thin film resistor

Visual inspection criteria for resistors is contained in TM 2032 . Section 3.1 Thin Film Resistors (100 to 200X) and Section 3.2 for Thick Film Resistors (10 to 60X).

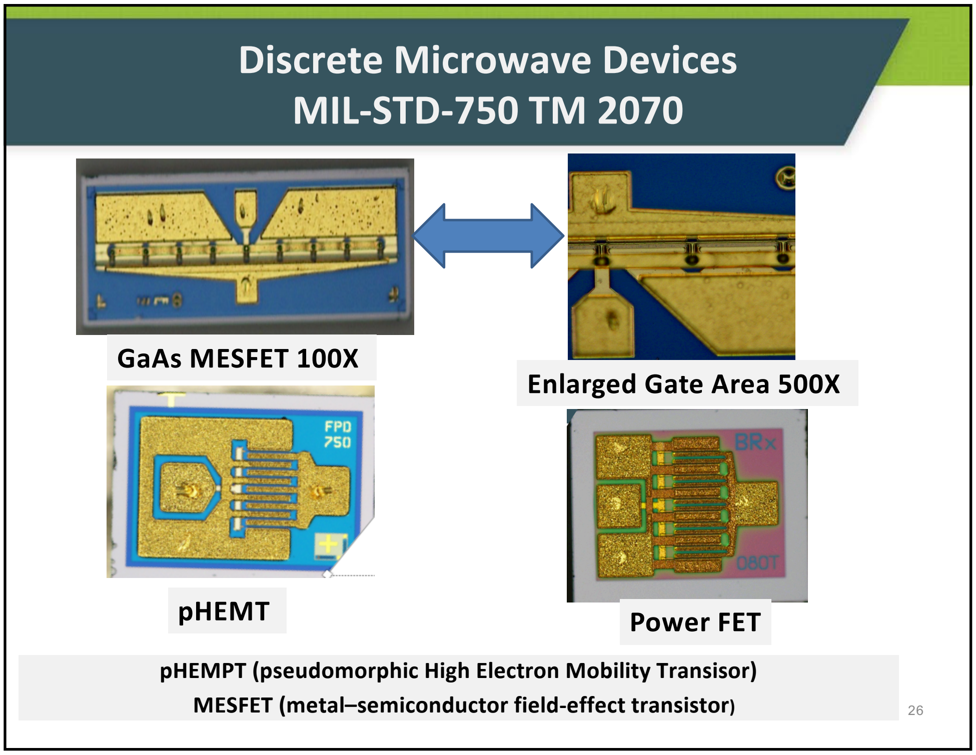
As with the capacitors component attach and wirebond criteria is found in TM 2017.

Course Notes



Component ID: Inductors Coils

Inductors are passive elements that resist instantaneous change in electrical flow by either building or collapsing an electric field. Standard unit of measure is the Henry H. Refer to TM 2032 Section 3.4 for inspection criteria for Inductors.



Discrete Microwave Devices
MIL-STD-750 TM 2070

GaAs MESFET 100X

Enlarged Gate Area 500X

pHEMT

Power FET

pHEMPT (pseudomorphic High Electron Mobility Transisor)

MESFET (metal–semiconductor field-effect transistor)

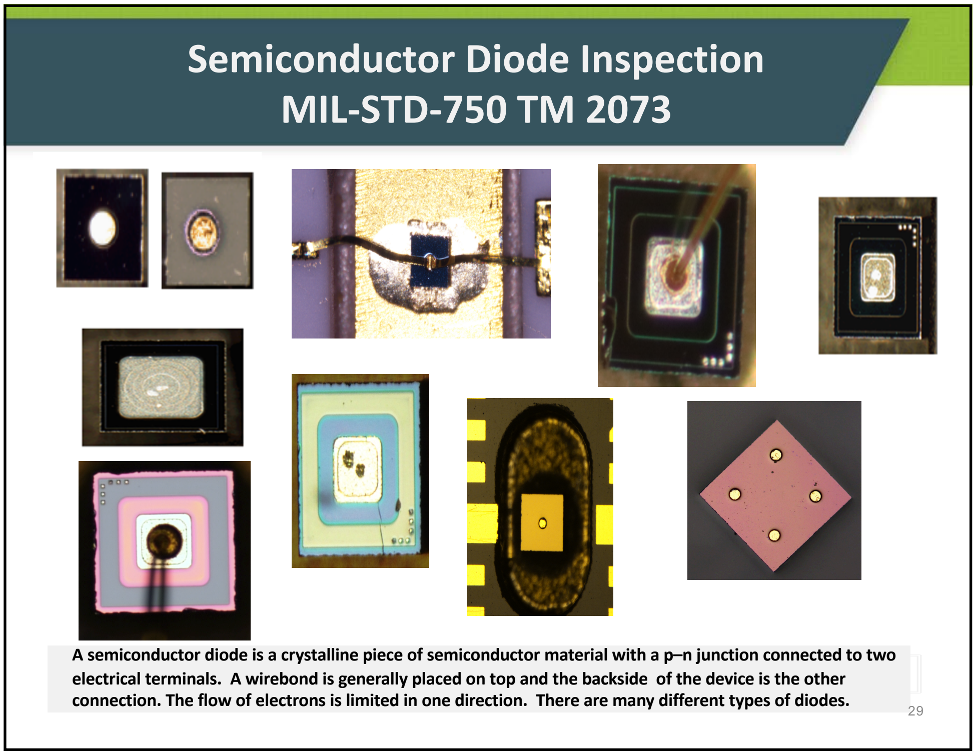
Course Notes

Transistors
MIL-STD-750 TM 2072

Typical Bipolar NPN transistors with a diffused guard rind surrounding the active area. The guard ring is like a moat around the castle designed to protect the sensitive gate regions from ions.
https://www.electronicshub.org/transistors-classification-and-types/

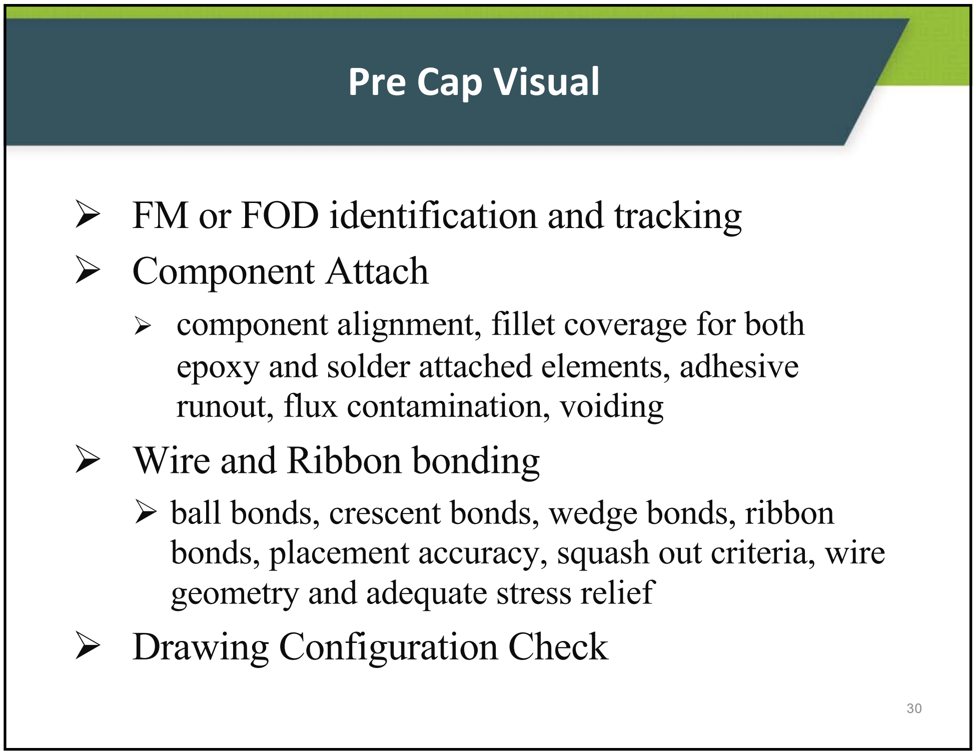
Power MOSFETS
MIL-STD-750 TM 2069

MOSFET in a TO 3 Package



Semiconductor Diode Inspection
MIL-STD-750 TM 2073

A semiconductor diode is a crystalline piece of semiconductor material with a p–n junction connected to two electrical terminals. A wirebond is generally placed on top and the backside of the device is the other connection. The flow of electrons is limited in one direction. There are many different types of diodes.



Pre Cap Visual

- FM or FOD identification and tracking
- Component Attach
  - component alignment, fillet coverage for both epoxy and solder attached elements, adhesive runout, flux contamination, voiding
- Wire and Ribbon bonding
  - ball bonds, crescent bonds, wedge bonds, ribbon bonds, placement accuracy, squash out criteria, wire geometry and adequate stress relief
- Drawing Configuration Check

Pre Cap Inspection Station

- Clean ESD controlled workstation
- Inspection is normally done under a well-lit laminar flow hood
- Class H requires Class 100,000 (Class 8 ISO 14644-1)
- Class K requires Class 100 (ISO Class 5)
- Maintain cleanroom classification between Pre Cap and Package seal
- Keep devices covered during transfer from one environment to another
- Relative humidity less that 65%
  - Usually a range is set e.g. 35 to 65 RH for ESD purposes

Foreign Material Contamination

Foreign Material Identification and Control

- Provision is intended to identify, control and eliminate foreign material that enters the manufacturing flow
- TM 2017 requires weekly audits for F/M...must identify nature and source of FM and take corrective action
- Unattached or partially attached F/M is a problem...can break loose and short two adjacent active conductive paths
- Residual flux, stains or surface contamination on the surface of an IC can cause corrosion and other problems
- Human spittle is ionic contamination and can lead to surface conduction in the presence of moisture

Foreign Material or F.O.D.

Definition...anything foreign to the process or displace material from a previous process step e.g. loose chips of silver epoxy and wire that are generated during rework can cause shorts.

- Need to assess **attached** vs. **unattached** or the threat of becoming unattached
- All foreign material shall be considered to be **unattached** unless otherwise verified to be attached
- The size of the particle relative to the shortest distance between two non-common conductors
- Liquid droplets or any chemical stain that bridges any combination of unglassivated or unpassivated active circuit areas

Foreign Material Mil Spec Requirements

The Primary source for FM/FOD criteria applicable at Pre Cap can be found at:

Hybrids (MIL-STD 883 TM 2017, para. 3.1.9)

There are additional referenced criteria (see Table 1) regarding FM/FOD applicable for particles on the surface of the IC/MMIC

Monolithics (MIL-STD 883 TM 2010, ¶3.2.5)

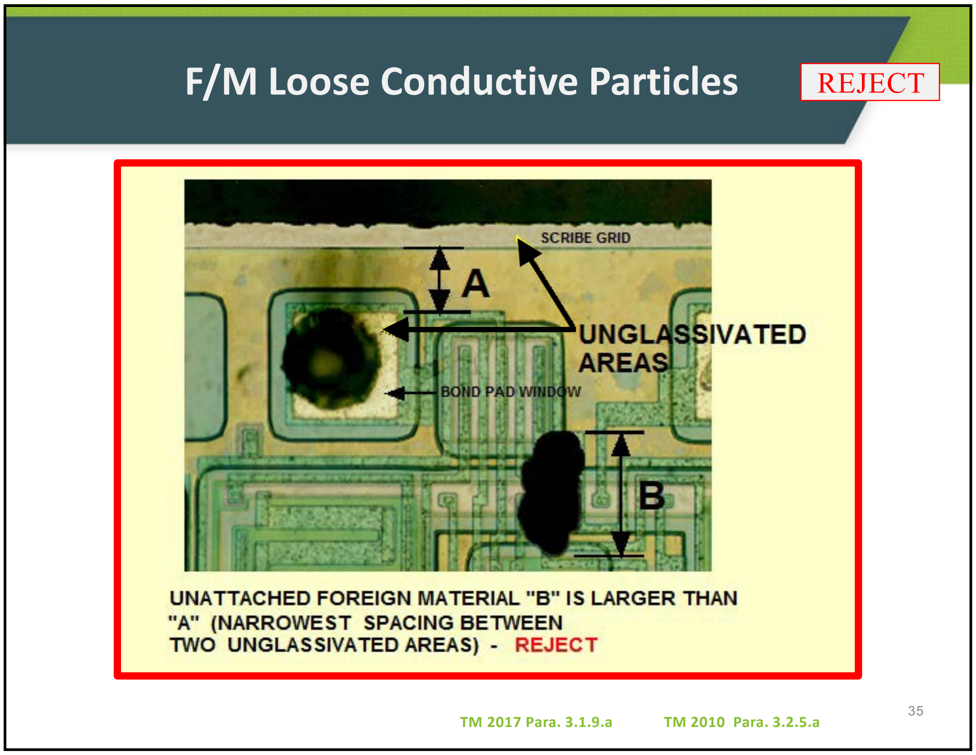
Passives (MIL-STD-883 TM 2032, ¶3.1.5 / 3.2.3)

Pre-cap Power MOSFETS (MIL-STD 750 TM 2069.2, ¶3.3.1)

Pre-cap Discrete and Multichip Transistors (MIL-STD-750 TM 2070.2, ¶3.6.1)

Internal Visual Transistor Inspection (MIL-STD-750 TM2072.8, ¶4.1.6)

Visual Inspection Of Die (MIL-STD-750 TM 2073.2, ¶4.3)

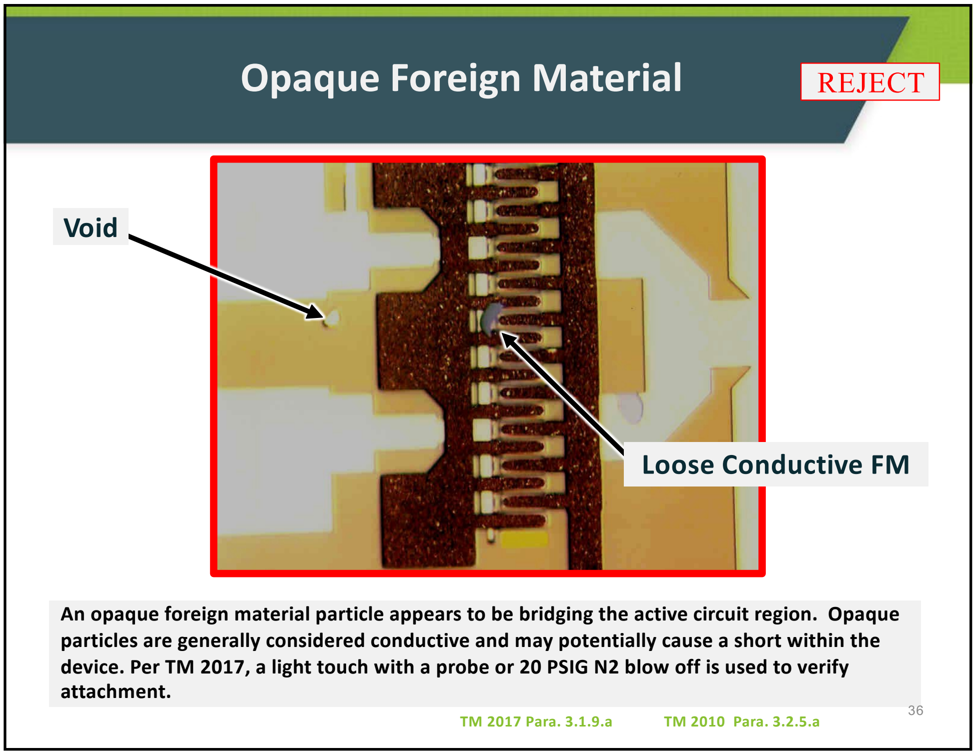


F/M Loose Conductive Particles

REJECT

UNATTACHED FOREIGN MATERIAL "B" IS LARGER THAN "A" (NARROWEST SPACING BETWEEN TWO UNGLASSIVATED AREAS) - REJECT

TM 2017 Para. 3.1.9.a TM 2010 Para. 3.2.5.a

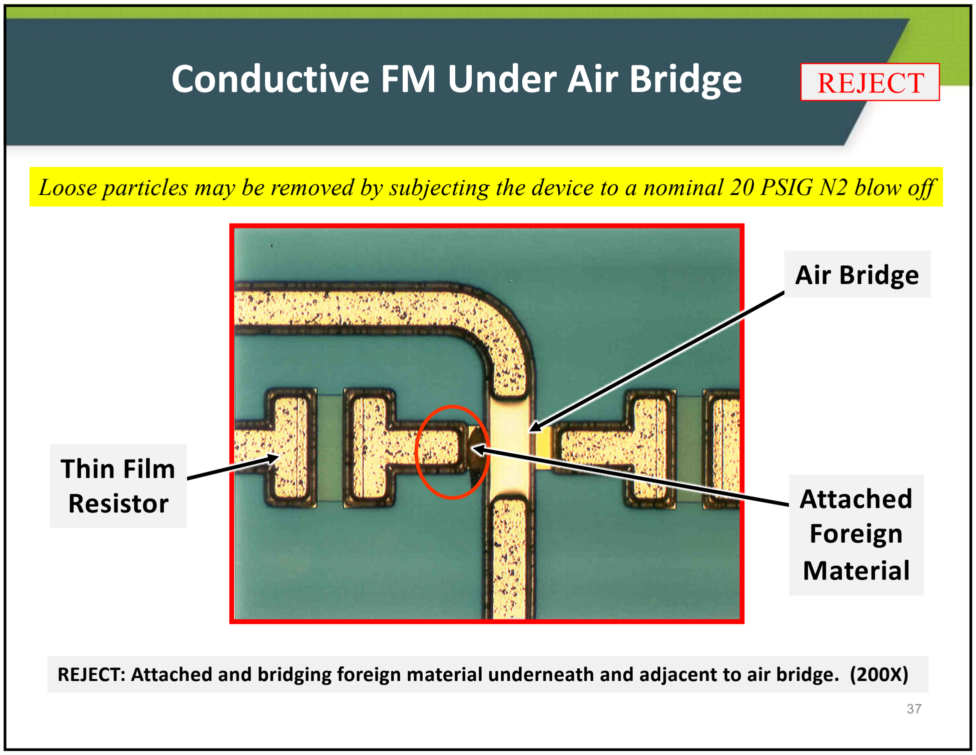


Opaque Foreign Material

REJECT

An opaque foreign material particle appears to be bridging the active circuit region. Opaque particles are generally considered conductive and may potentially cause a short within the device. Per TM 2017, a light touch with a probe or 20 PSIG N2 blow off is used to verify attachment.

TM 2017 Para. 3.1.9.a TM 2010 Para. 3.2.5.a

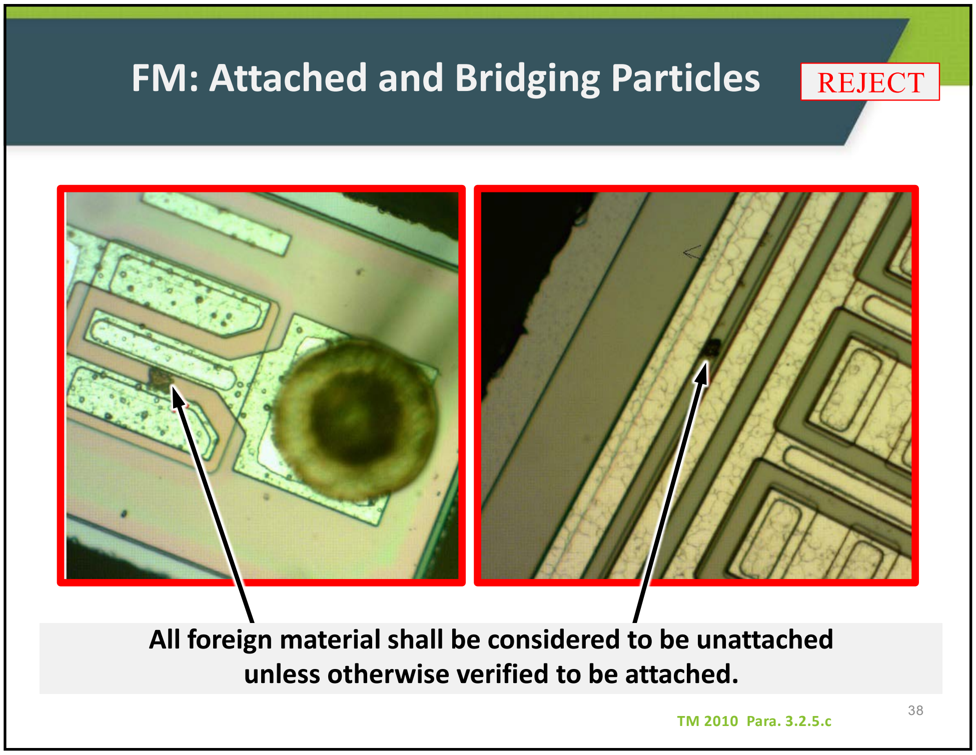


Conductive FM Under Air Bridge

REJECT

Loose particles may be removed by subjecting the device to a nominal 20 PSIG N2 blow off

REJECT: Attached and bridging foreign material underneath and adjacent to air bridge. (200X)



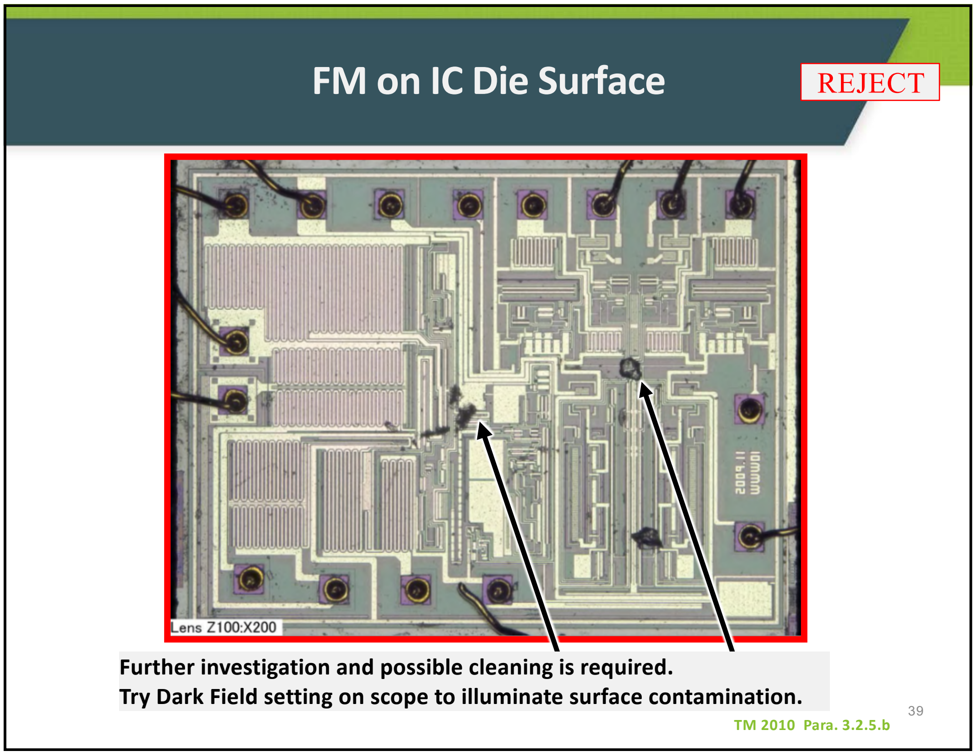
FM: Attached and Bridging Particles

REJECT

All foreign material shall be considered to be unattached unless otherwise verified to be attached.

TM 2010 Para. 3.2.5.c

Course Notes

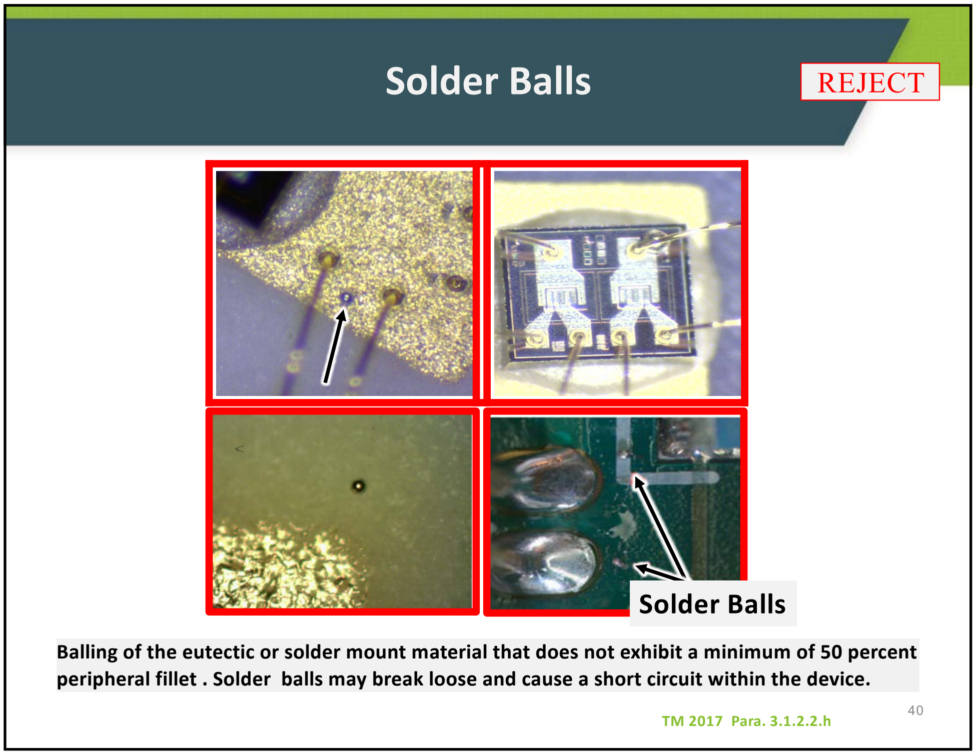


FM on IC Die Surface

REJECT

Further investigation and possible cleaning is required.
Try Dark Field setting on scope to illuminate surface contamination.

TM 2010 Para. 3.2.5.b



Solder Balls

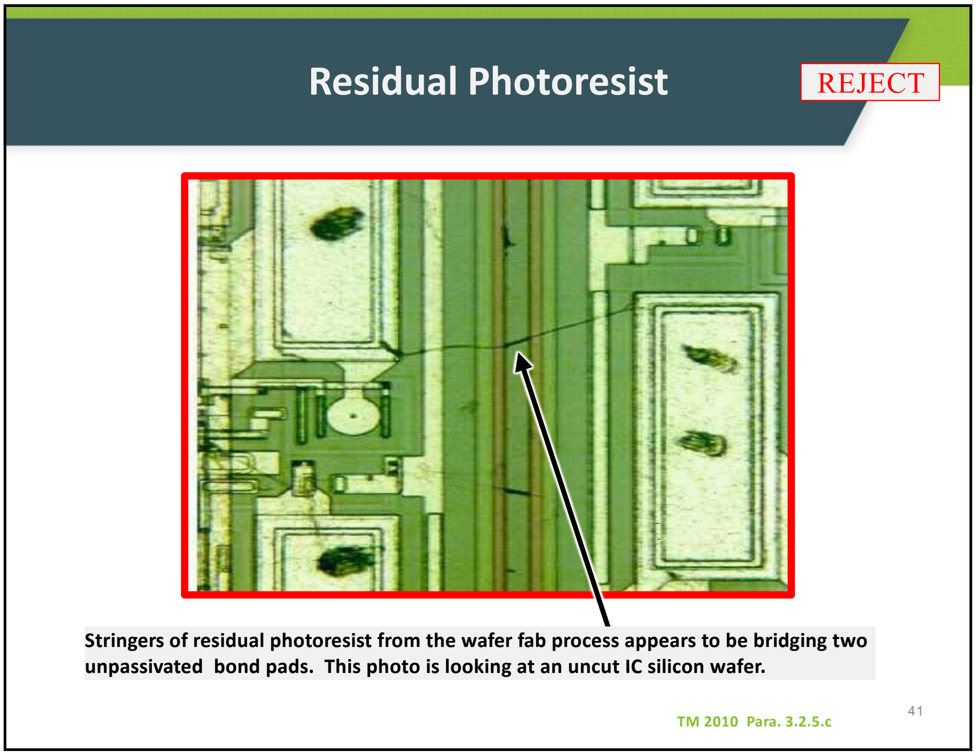
REJECT

Solder Balls

Balling of the eutectic or solder mount material that does not exhibit a minimum of 50 percent peripheral fillet . Solder balls may break loose and cause a short circuit within the device.

TM 2017 Para. 3.1.2.2.h

Course Notes

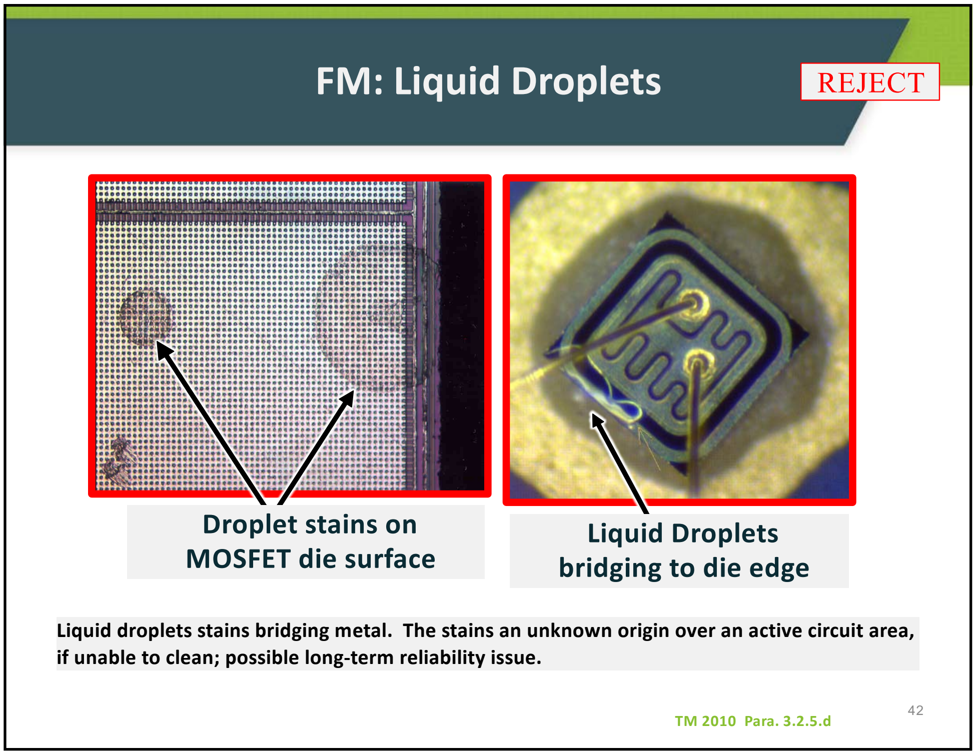


Residual Photoresist

REJECT

Stringers of residual photoresist from the wafer fab process appears to be bridging two unpassivated bond pads. This photo is looking at an uncut IC silicon wafer.

TM 2010 Para. 3.2.5.c



FM: Liquid Droplets

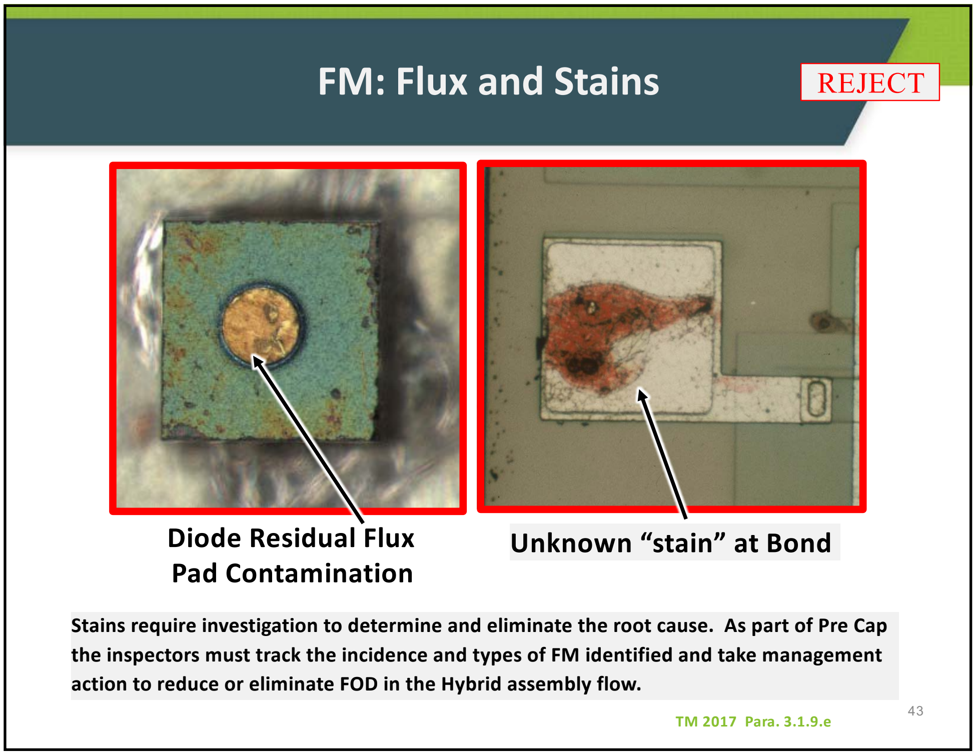
REJECT

Droplet stains on MOSFET die surface

Liquid Droplets bridging to die edge

Liquid droplets stains bridging metal. The stains an unknown origin over an active circuit area, if unable to clean; possible long-term reliability issue.

TM 2010 Para. 3.2.5.d



FM: Flux and Stains

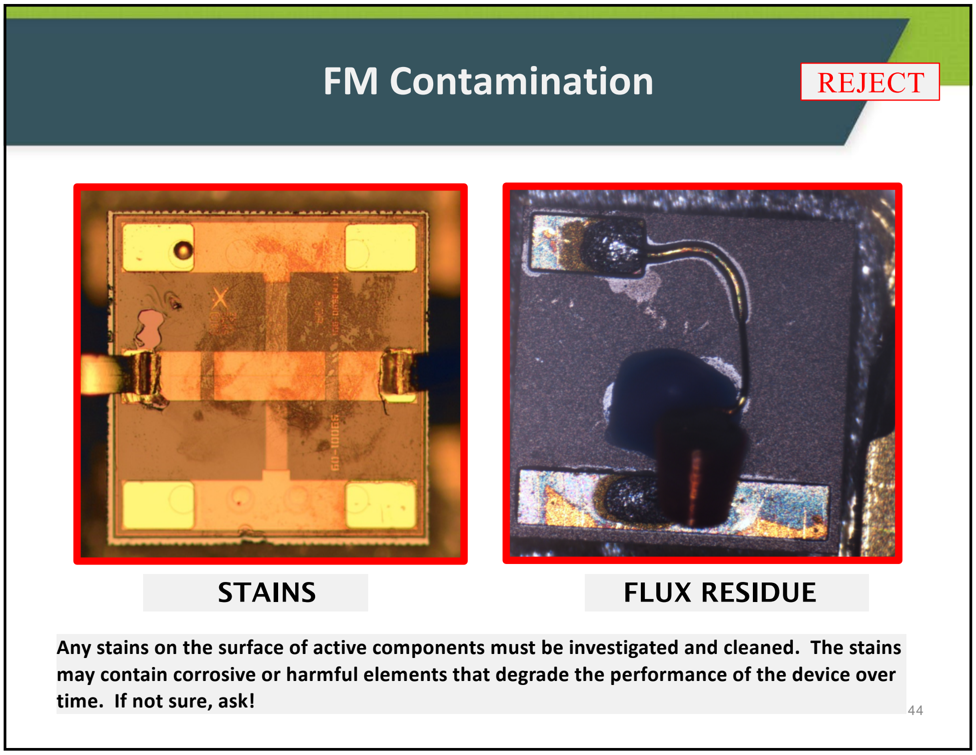
REJECT

Diode Residual Flux Pad Contamination

Unknown “stain” at Bond

Stains require investigation to determine and eliminate the root cause. As part of Pre Cap the inspectors must track the incidence and types of FM identified and take management action to reduce or eliminate FOD in the Hybrid assembly flow.

TM 2017 Para. 3.1.9.e



FM Contamination

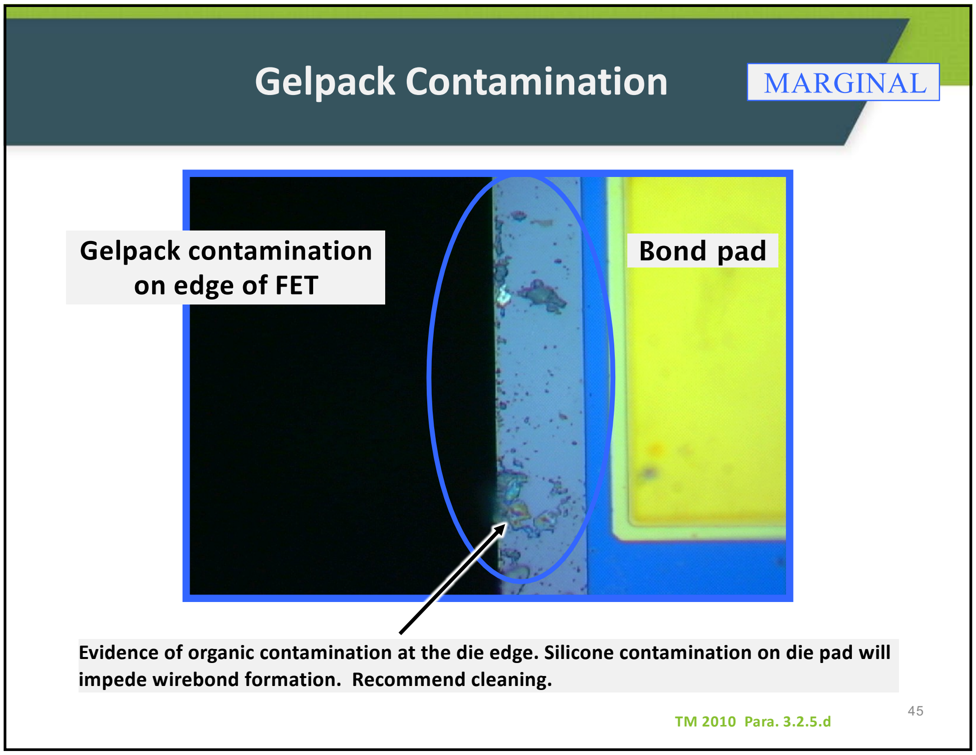
REJECT

STAINS

FLUX RESIDUE

Any stains on the surface of active components must be investigated and cleaned. The stains may contain corrosive or harmful elements that degrade the performance of the device over time. If not sure, ask!

Course Notes



Gelpack Contamination

MARGINAL

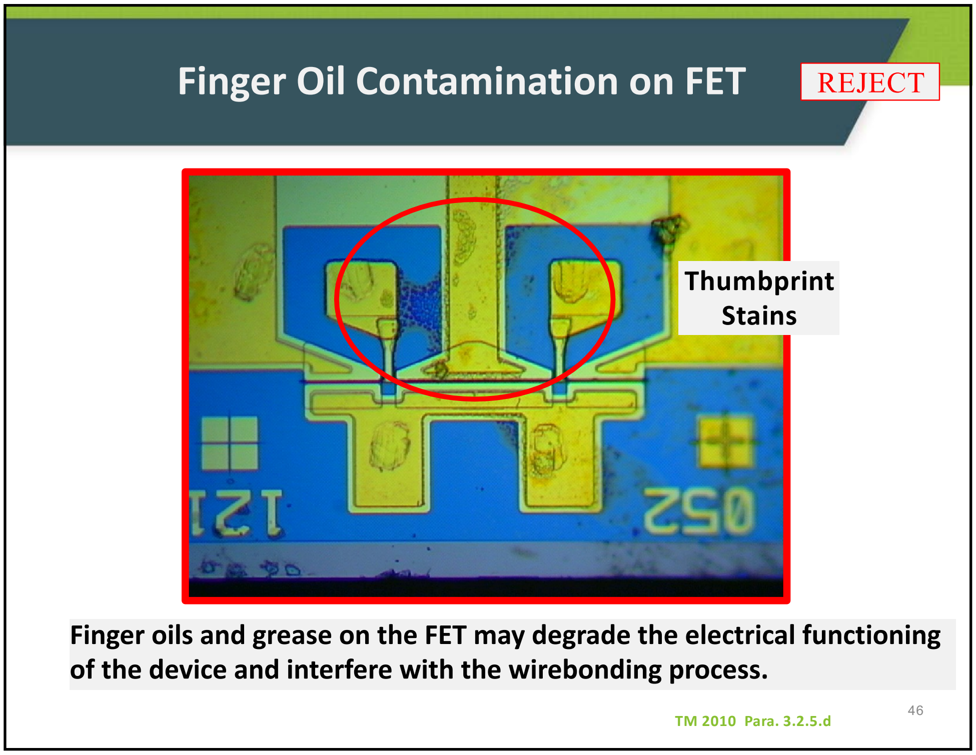
Gelpack contamination on edge of FET

Bond pad

Evidence of organic contamination at the die edge. Silicone contamination on die pad will impede wirebond formation. Recommend cleaning.

TM 2010 Para. 3.2.5.d

45



Finger Oil Contamination on FET

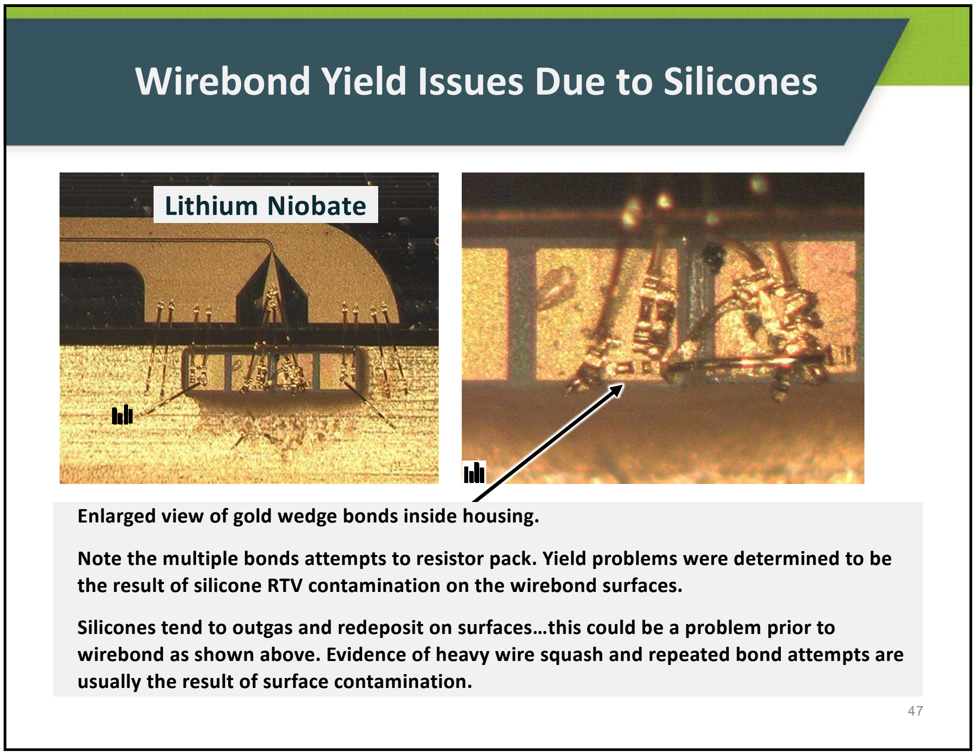
REJECT

Thumbprint Stains

Finger oils and grease on the FET may degrade the electrical functioning of the device and interfere with the wirebonding process.

TM 2010 Para. 3.2.5.d

46

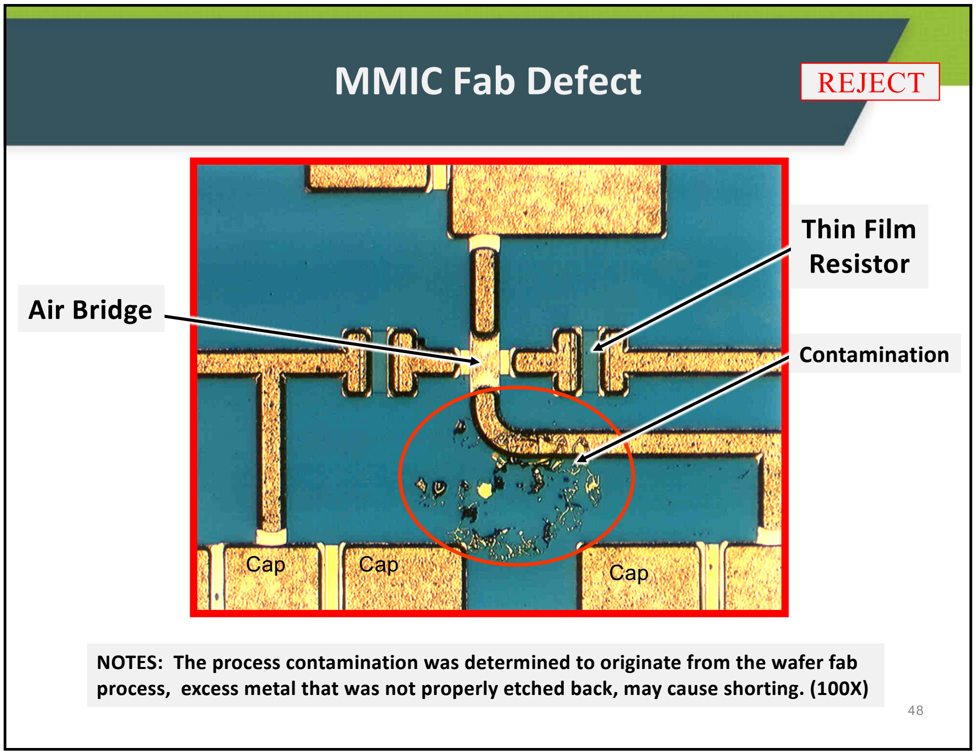


Wirebond Yield Issues Due to Silicones

Enlarged view of gold wedge bonds inside housing.

Note the multiple bonds attempts to resistor pack. Yield problems were determined to be the result of silicone RTV contamination on the wirebond surfaces.

Silicones tend to outgas and redeposit on surfaces…this could be a problem prior to wirebond as shown above. Evidence of heavy wire squash and repeated bond attempts are usually the result of surface contamination.

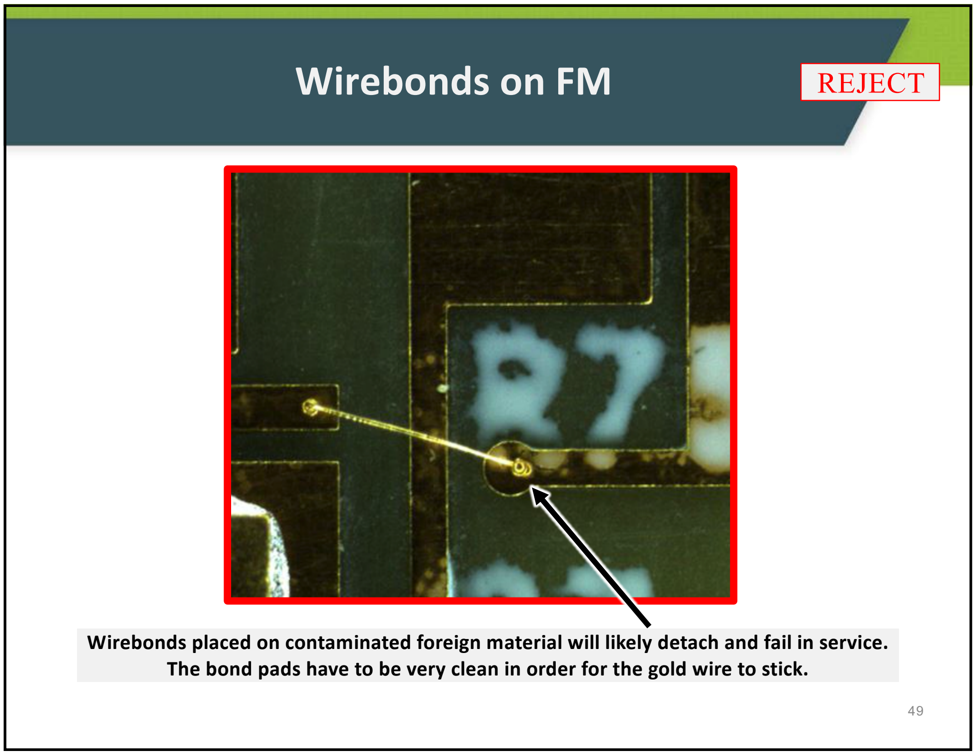


MMIC Fab Defect

REJECT

NOTES: The process contamination was determined to originate from the wafer fab process, excess metal that was not properly etched back, may cause shorting. (100X)

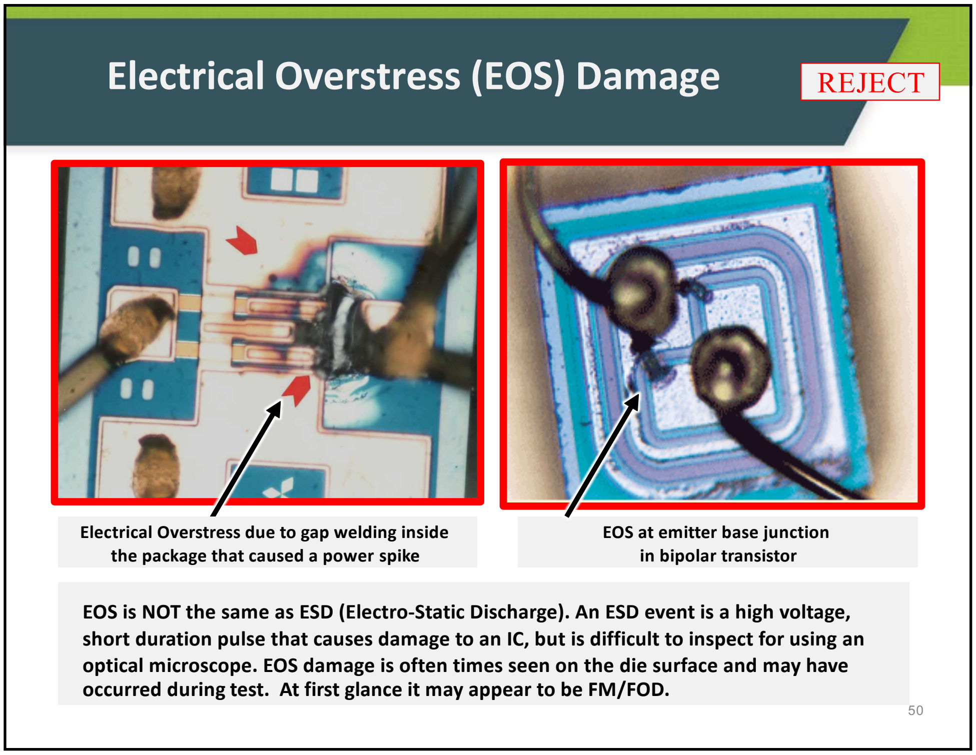
Course Notes



Wirebonds on FM

REJECT

Wirebonds placed on contaminated foreign material will likely detach and fail in service. The bond pads have to be very clean in order for the gold wire to stick.



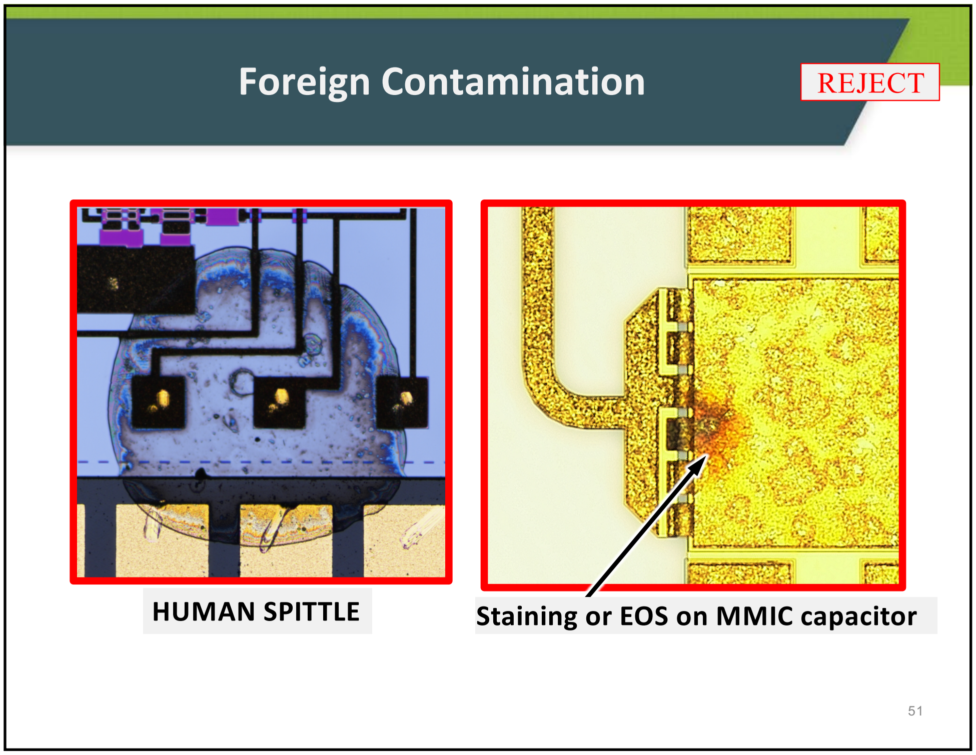
Electrical Overstress (EOS) Damage

REJECT

Electrical Overstress due to gap welding inside the package that caused a power spike

EOS at emitter base junction in bipolar transistor

EOS is NOT the same as ESD (Electro-Static Discharge). An ESD event is a high voltage, short duration pulse that causes damage to an IC, but is difficult to inspect for using an optical microscope. EOS damage is often times seen on the die surface and may have occurred during test. At first glance it may appear to be FM/FOD.

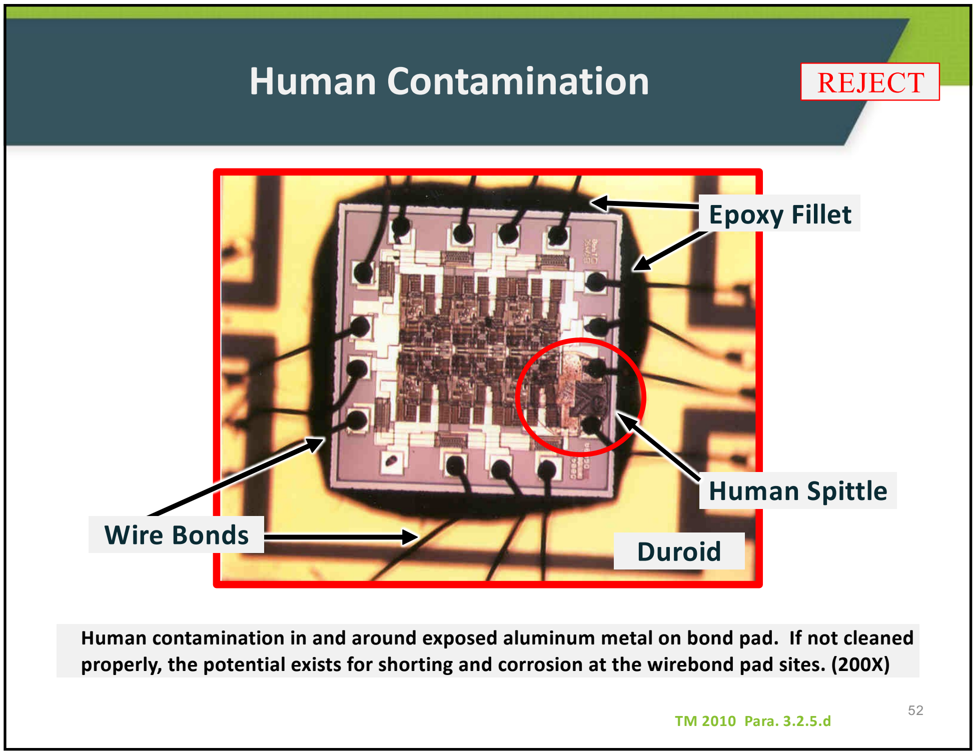


Foreign Contamination

REJECT

HUMAN SPITTLE

Staining or EOS on MMIC capacitor



Human Contamination

REJECT

Human contamination in and around exposed aluminum metal on bond pad. If not cleaned properly, the potential exists for shorting and corrosion at the wirebond pad sites. (200X)

TM 2010 Para. 3.2.5.d

Space Shuttle Launch Abort Due to Spittle

SPITTLE VIDEO

- In 1984 a Space Shuttle launch had to abort in the final countdown because of a failure of an IC in an on-board computer.
- After an extensive FA investigation the root cause of failure was traced to human contamination that had dried onto the surface of the IC and caused corrosion and an open circuit condition.
- Spittle and other forms of organic contaminants contain ions such as chlorine (Cl) and potassium (K) and sodium (Na), which combine with moisture to corrode aluminum metal.
- Identification and elimination of human contamination inside a hybrid is part of the inspection process

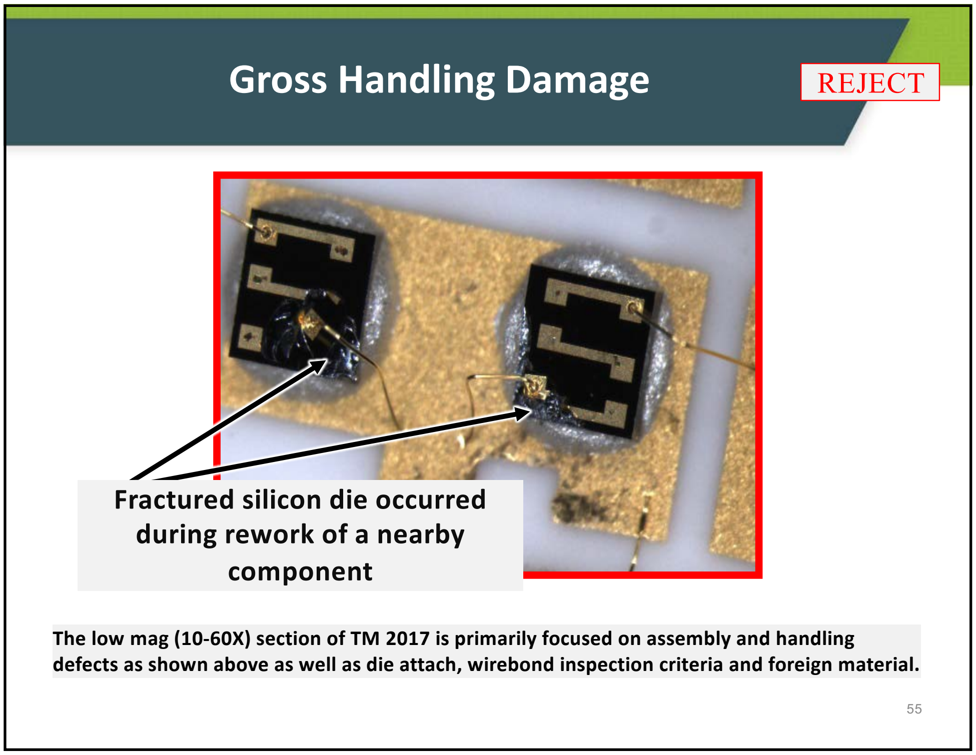
Hybrid Low Mag Inspect (10 to 60X)

Stereo Zoom Microscope

Inspect for die attach, wire and ribbon bond, F/M and assembly related defects. Must be able to handle and freely rotate the part under the microscope.

Use finger cots or gloves and follow ESD safe handling procedures .

A formal “Pre Cap”, sometimes in the presence of the customer is the last and most important visual inspection step prior to hermetic seal. No further process steps are allowed after the final inspection.



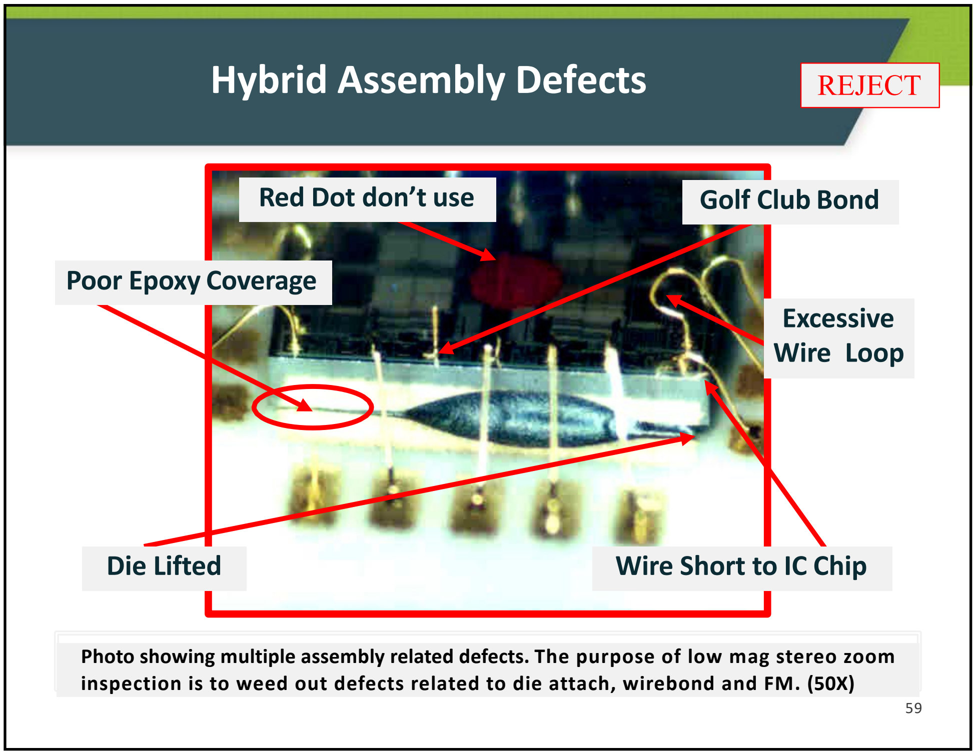
Gross Handling Damage

REJECT

Fractured silicon die occurred during rework of a nearby component

The low mag (10-60X) section of TM 2017 is primarily focused on assembly and handling defects as shown above as well as die attach, wirebond inspection criteria and foreign material.

55



Hybrid Assembly Defects

REJECT

Red Dot don’t use

Golf Club Bond

Poor Epoxy Coverage

Excessive Wire Loop

Die Lifted

Wire Short to IC Chip

Photo showing multiple assembly related defects. The purpose of low mag stereo zoom inspection is to weed out defects related to die attach, wirebond and FM. (50X)

56

Die Attach Inspection

ICs and MMICs are often glued down using dispensed adhesives such as silver (Ag) filled epoxy or non-conductive (white) epoxy

- Evidence of a fillet around the perimeter of the die is an indication that the die is well attached
- If epoxy is put down as a film or dispensed in a needle on an automatic machine the fillet requirement can be met by an inspection step prior assuring 75% area coverage on the pad

High powered MOSFETS and semiconductors are often soldered into place using “eutectic” solder alloys e.g. Gold Tin (AuSn)

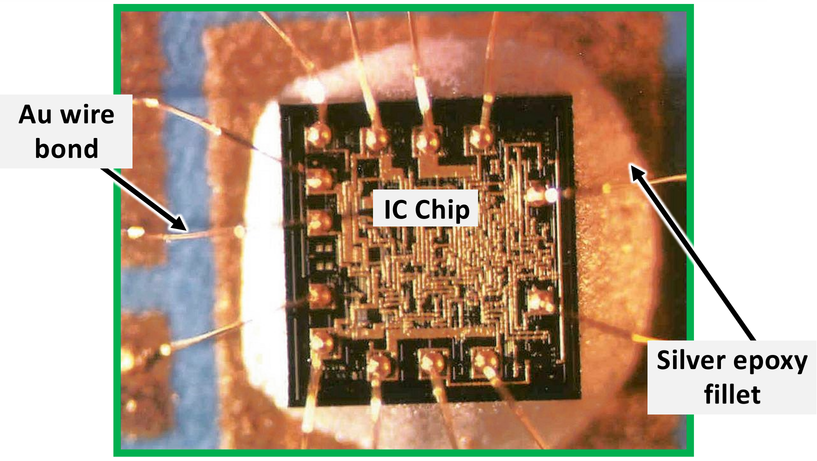
- Evidence of eutectic solder runout around the perimeter looks different than a fillet of epoxy that will climb up the side of the die edge. However, the perimeter coverage criteria is the same.

After die attach it’s important to inspect for:

- Surface flatness of the IC/MMIC is very important along with cleanliness of the bonding surface
- Excess epoxy or resin bleed out from the epoxy. Wirebonding to resin bleed is not allowed
- Contamination of the bonding surfaces due to the oven cure process etc.
- Discoloration of the package plating due to thin or contaminated gold surfaces

Silicon Chip Hand Mounted

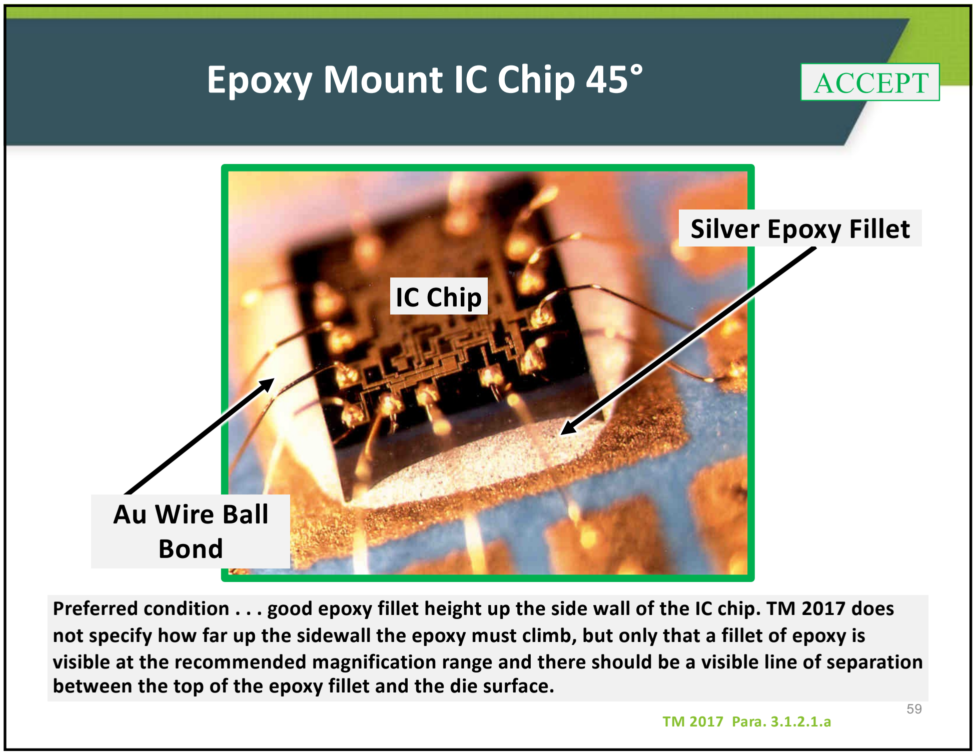
ACCEPT



Preferred condition, IC component attach with good coverage of silver epoxy fillet on all four sides. View is looking directly down on the IC.

TM 2017 Para. 3.1.2.1.a

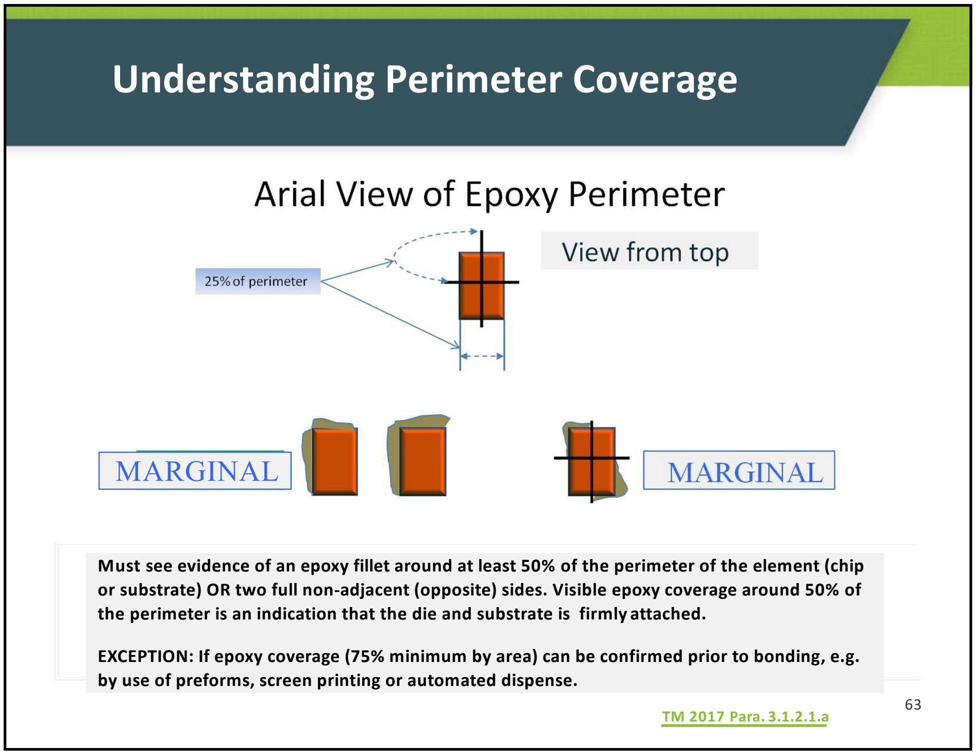
Course Notes



Epoxy Mount IC Chip 45°

Preferred condition . . . good epoxy fillet height up the side wall of the IC chip. TM 2017 does not specify how far up the sidewall the epoxy must climb, but only that a fillet of epoxy is visible at the recommended magnification range and there should be a visible line of separation between the top of the epoxy fillet and the die surface.

TM 2017 Para. 3.1.2.1.a



Understanding Perimeter Coverage

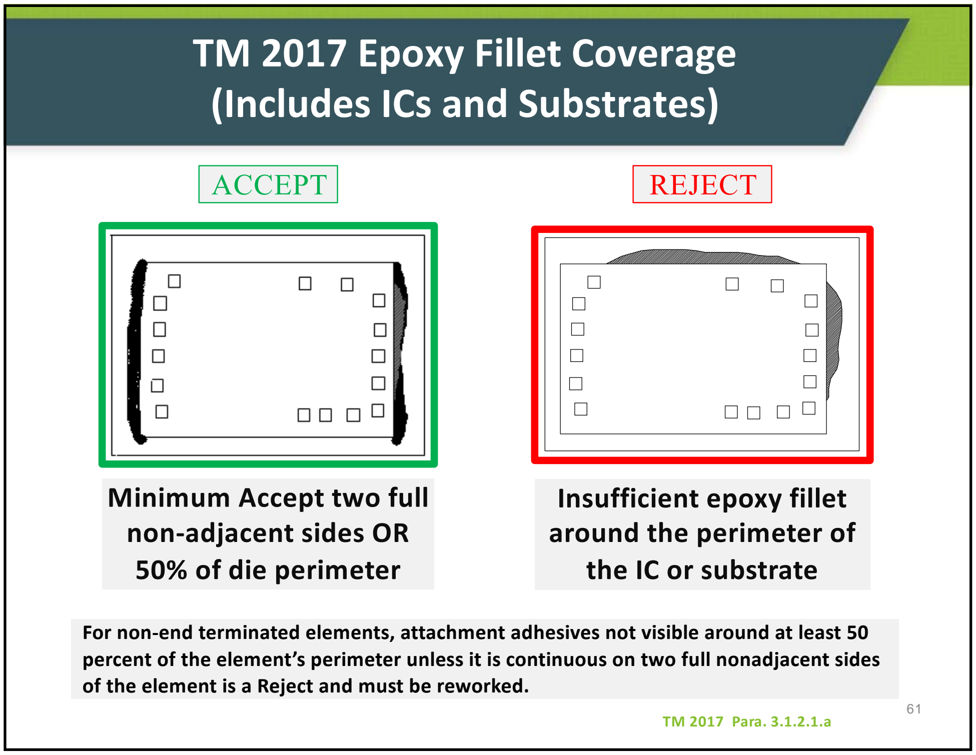
Arial View of Epoxy Perimeter

Must see evidence of an epoxy fillet around at least 50% of the perimeter of the element (chip or substrate) OR two full non-adjacent (opposite) sides. Visible epoxy coverage around 50% of the perimeter is an indication that the die and substrate is firmly attached.

EXCEPTION: If epoxy coverage (75% minimum by area) can be confirmed prior to bonding, e.g. by use of preforms, screen printing or automated dispense.

TM 2017 Para. 3.1.2.1.a

Course Notes



TM 2017 Epoxy Fillet Coverage (Includes ICs and Substrates)

ACCEPT

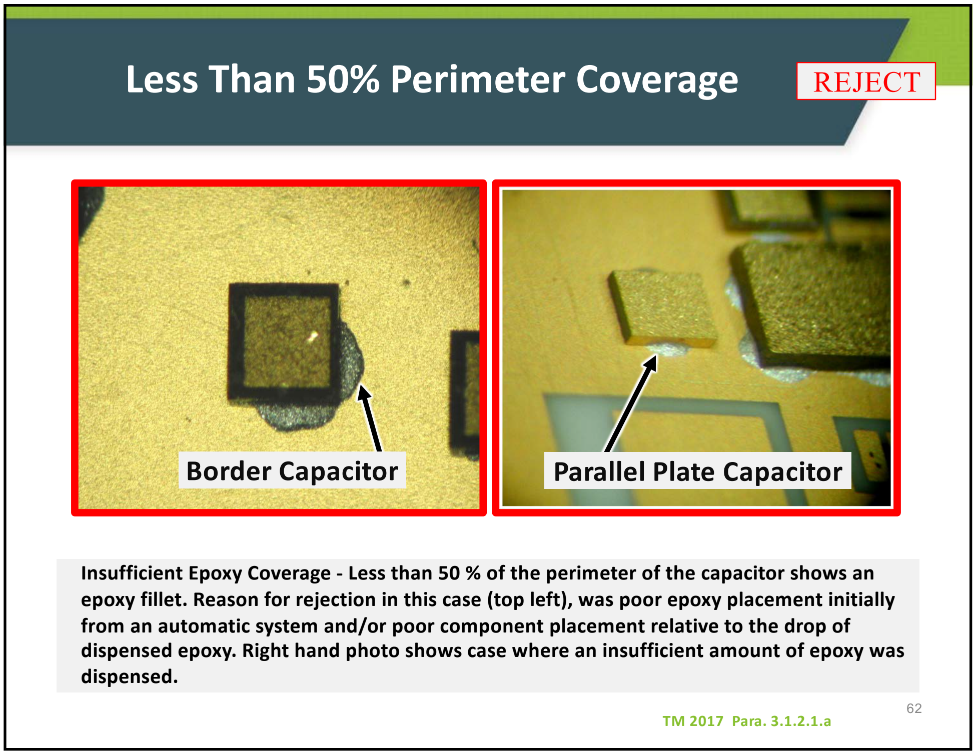
REJECT

Minimum Accept two full non-adjacent sides OR 50% of die perimeter

Insufficient epoxy fillet around the perimeter of the IC or substrate

For non-end terminated elements, attachment adhesives not visible around at least 50 percent of the element's perimeter unless it is continuous on two full nonadjacent sides of the element is a Reject and must be reworked.

TM 2017 Para. 3.1.2.1.a



Less Than 50% Perimeter Coverage

REJECT

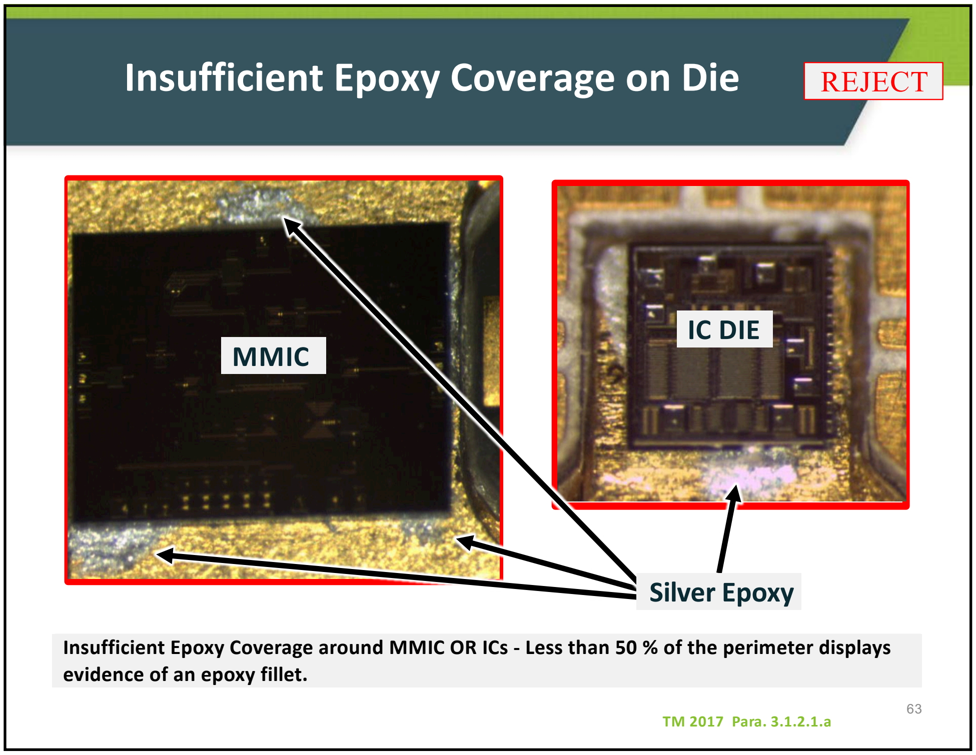
Border Capacitor

Parallel Plate Capacitor

Insufficient Epoxy Coverage - Less than 50 % of the perimeter of the capacitor shows an epoxy fillet. Reason for rejection in this case (top left), was poor epoxy placement initially from an automatic system and/or poor component placement relative to the drop of dispensed epoxy. Right hand photo shows case where an insufficient amount of epoxy was dispensed.

TM 2017 Para. 3.1.2.1.a

Course Notes

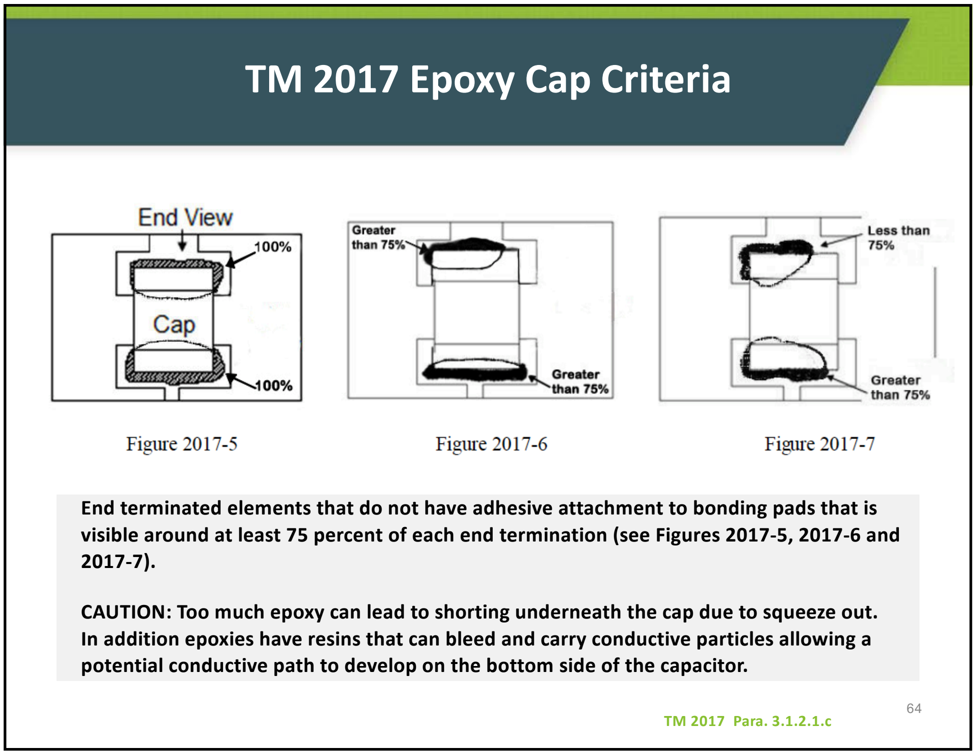


Insufficient Epoxy Coverage on Die

REJECT

Insufficient Epoxy Coverage around MMIC OR ICs - Less than 50 % of the perimeter displays evidence of an epoxy fillet.

TM 2017 Para. 3.1.2.1.a



TM 2017 Epoxy Cap Criteria

Figure 2017-5

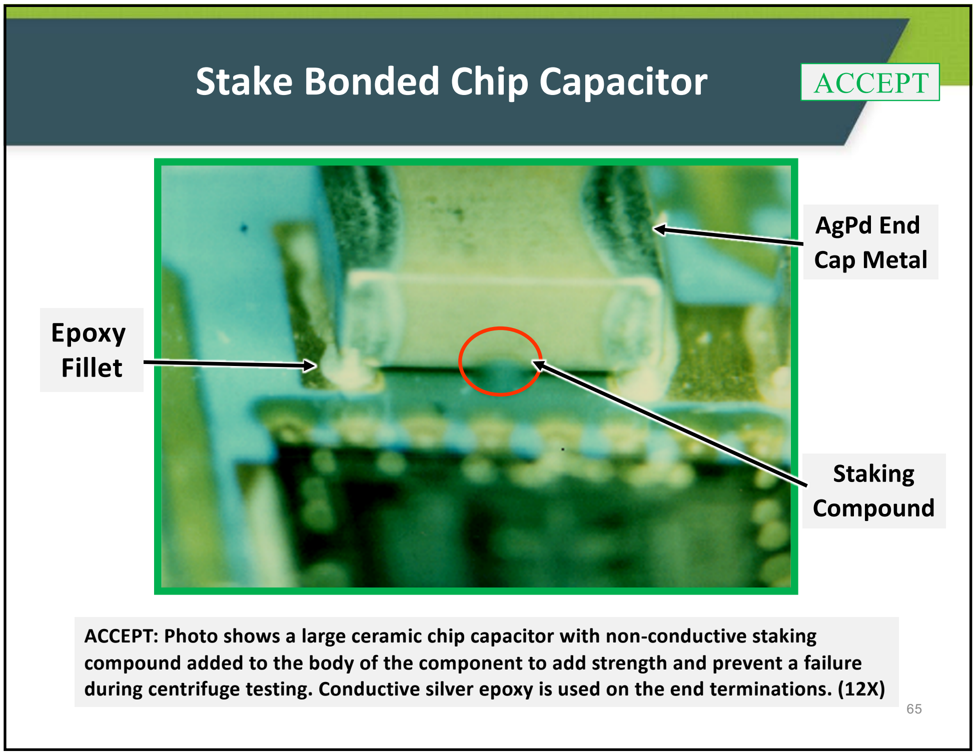
Figure 2017-6

Figure 2017-7

End terminated elements that do not have adhesive attachment to bonding pads that is visible around at least 75 percent of each end termination (see Figures 2017-5, 2017-6 and 2017-7).

CAUTION: Too much epoxy can lead to shorting underneath the cap due to squeeze out. In addition epoxies have resins that can bleed and carry conductive particles allowing a potential conductive path to develop on the bottom side of the capacitor.

TM 2017 Para. 3.1.2.1.c



Stake Bonded Chip Capacitor

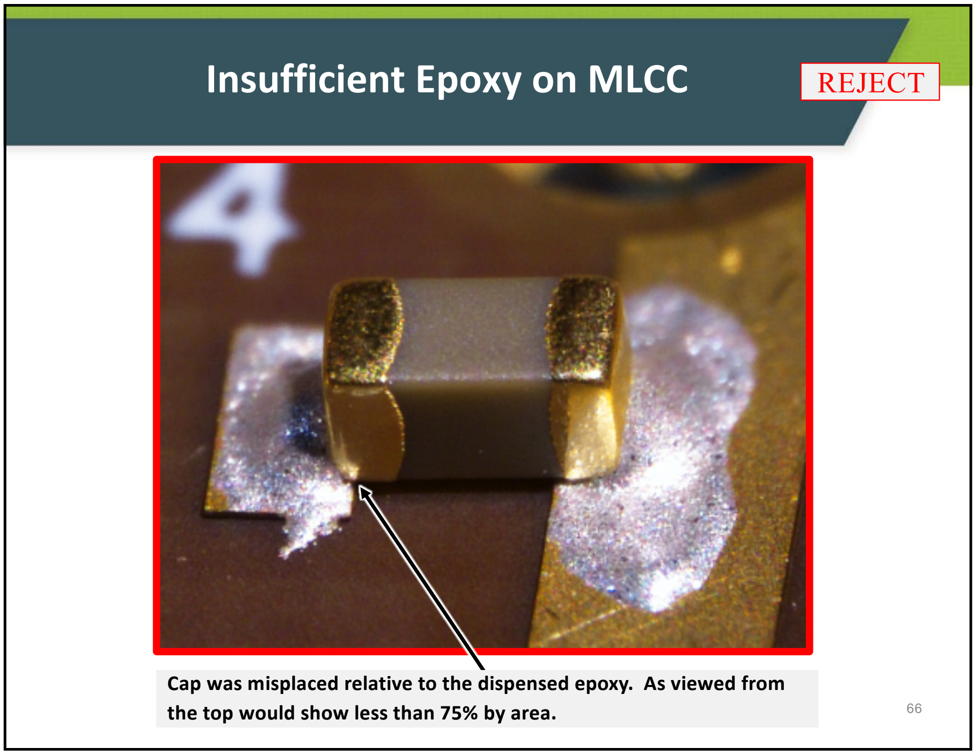
ACCEPT

Epoxy Fillet

AgPd End Cap Metal

Staking Compound

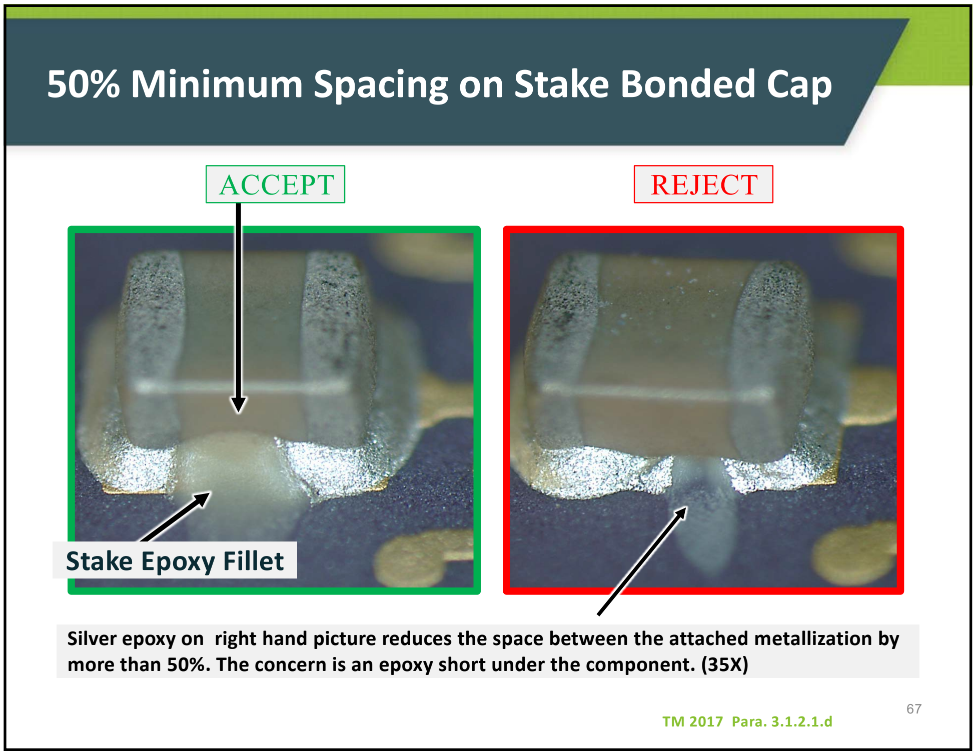
ACCEPT: Photo shows a large ceramic chip capacitor with non-conductive staking compound added to the body of the component to add strength and prevent a failure during centrifuge testing. Conductive silver epoxy is used on the end terminations. (12X)



Insufficient Epoxy on MLCC

REJECT

Cap was misplaced relative to the dispensed epoxy. As viewed from the top would show less than 75% by area.



50% Minimum Spacing on Stake Bonded Cap

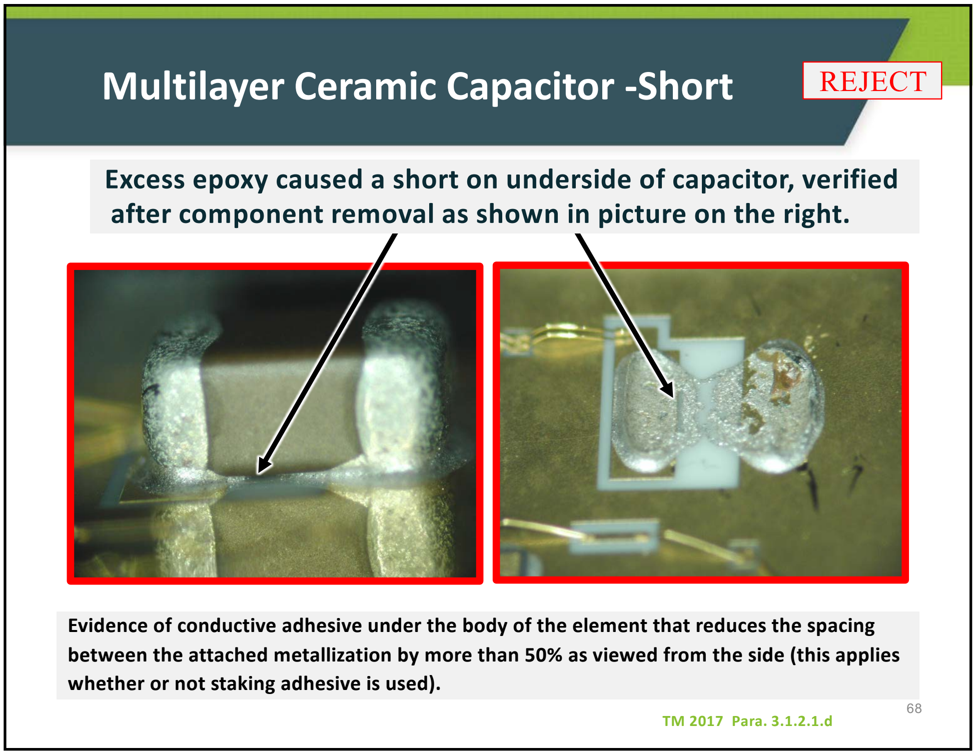
ACCEPT

REJECT

Stake Epoxy Fillet

Silver epoxy on right hand picture reduces the space between the attached metallization by more than 50%. The concern is an epoxy short under the component. (35X)

TM 2017 Para. 3.1.2.1.d



Multilayer Ceramic Capacitor -Short

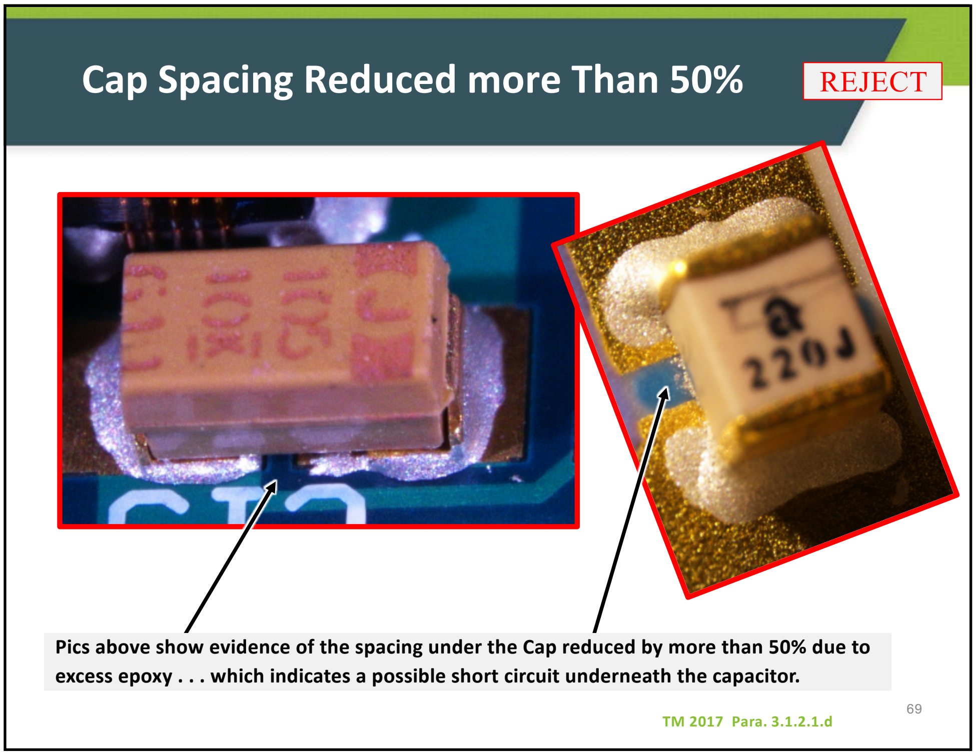
REJECT

Excess epoxy caused a short on underside of capacitor, verified after component removal as shown in picture on the right.

Evidence of conductive adhesive under the body of the element that reduces the spacing between the attached metallization by more than 50% as viewed from the side (this applies whether or not staking adhesive is used).

TM 2017 Para. 3.1.2.1.d

Course Notes



Cap Spacing Reduced more Than 50%

REJECT

Pics above show evidence of the spacing under the Cap reduced by more than 50% due to excess epoxy . . . which indicates a possible short circuit underneath the capacitor.

TM 2017 Para. 3.1.2.1.d

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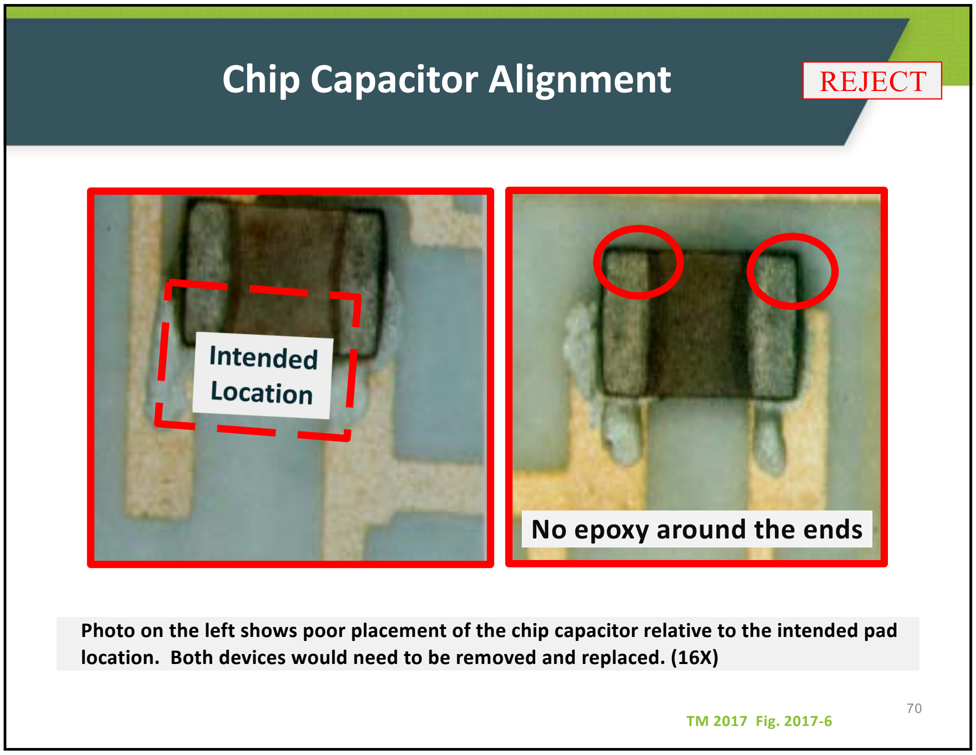


Chip Capacitor Alignment

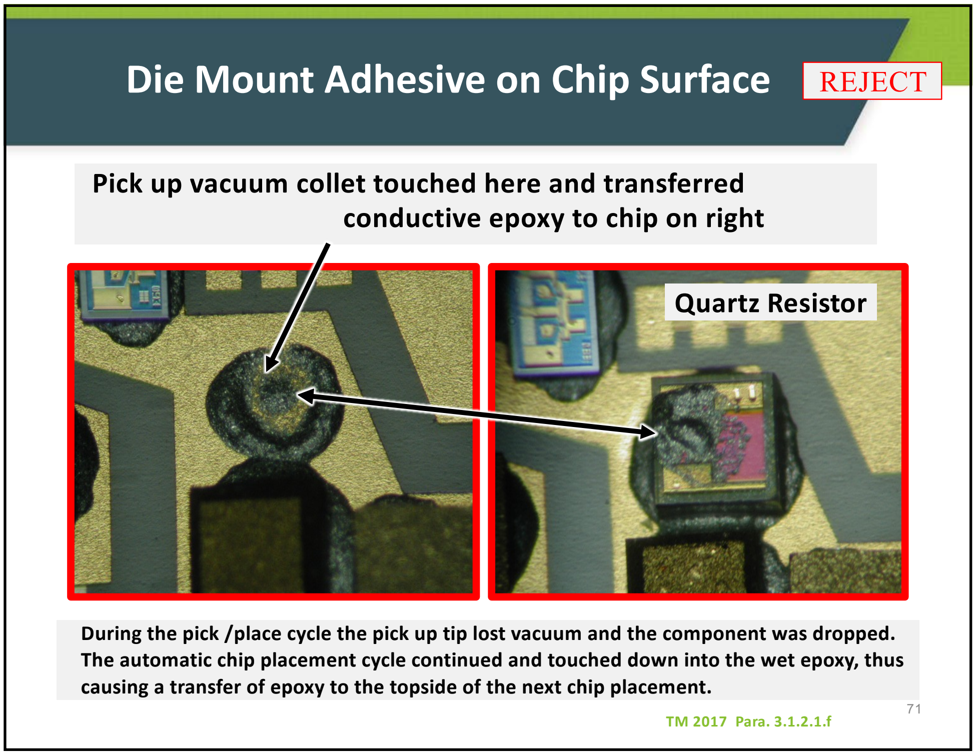
REJECT

Photo on the left shows poor placement of the chip capacitor relative to the intended pad location. Both devices would need to be removed and replaced. (16X)

TM 2017 Fig. 2017-6

70

Course Notes



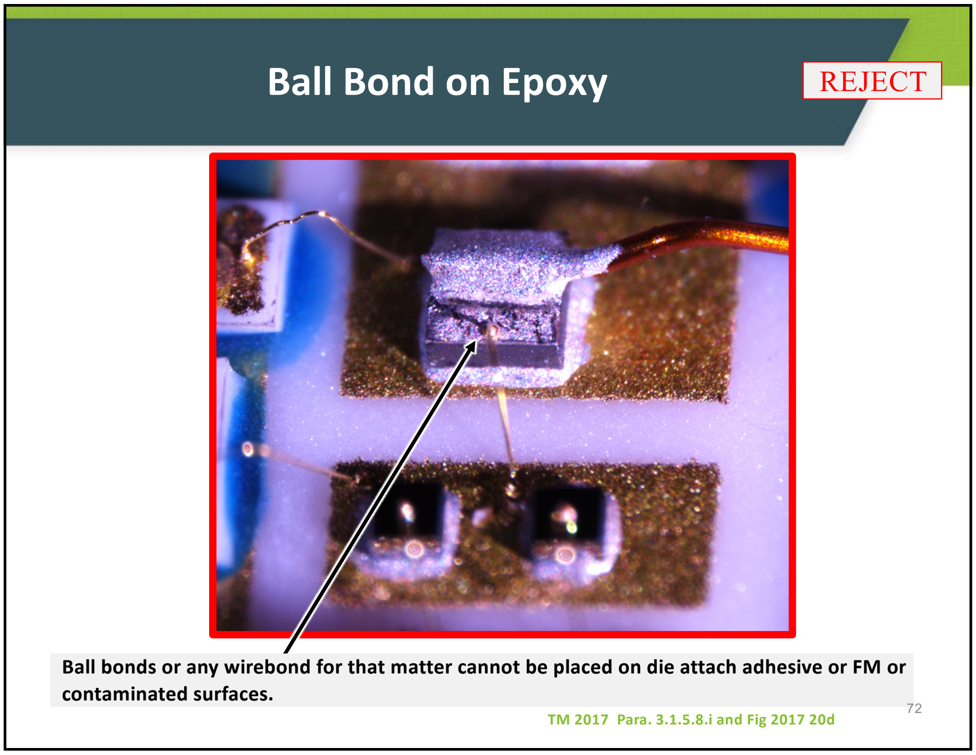
Die Mount Adhesive on Chip Surface

REJECT

Pick up vacuum collet touched here and transferred conductive epoxy to chip on right

During the pick /place cycle the pick up tip lost vacuum and the component was dropped. The automatic chip placement cycle continued and touched down into the wet epoxy, thus causing a transfer of epoxy to the topside of the next chip placement.

TM 2017 Para. 3.1.2.1.f

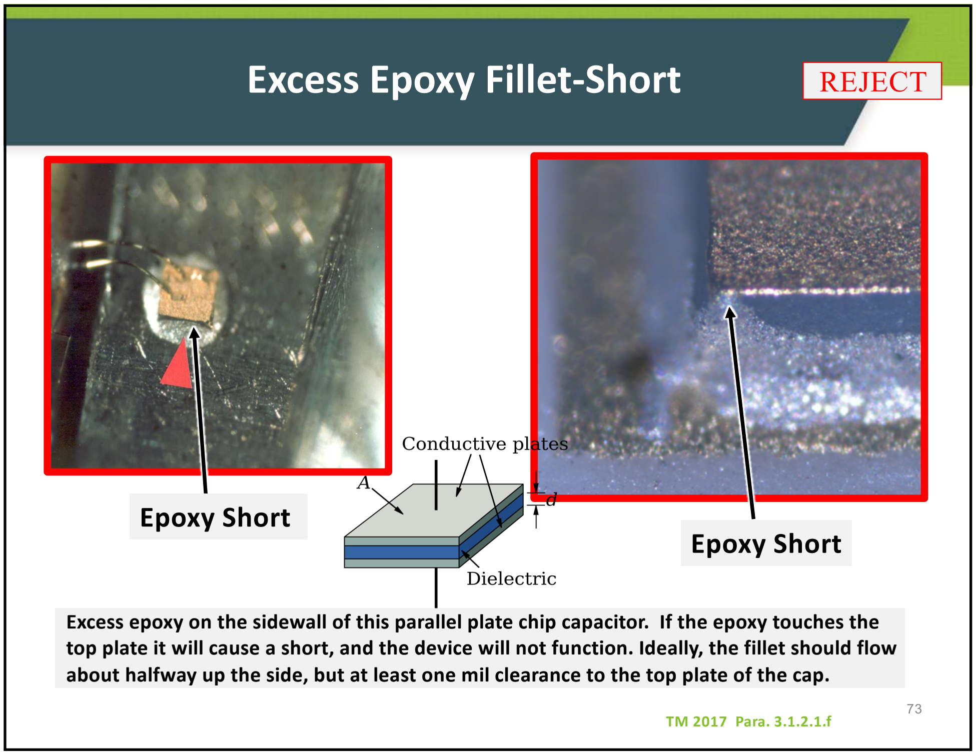


Ball Bond on Epoxy

REJECT

Ball bonds or any wirebond for that matter cannot be placed on die attach adhesive or FM or contaminated surfaces.

TM 2017 Para. 3.1.5.8.i and Fig 2017 20d



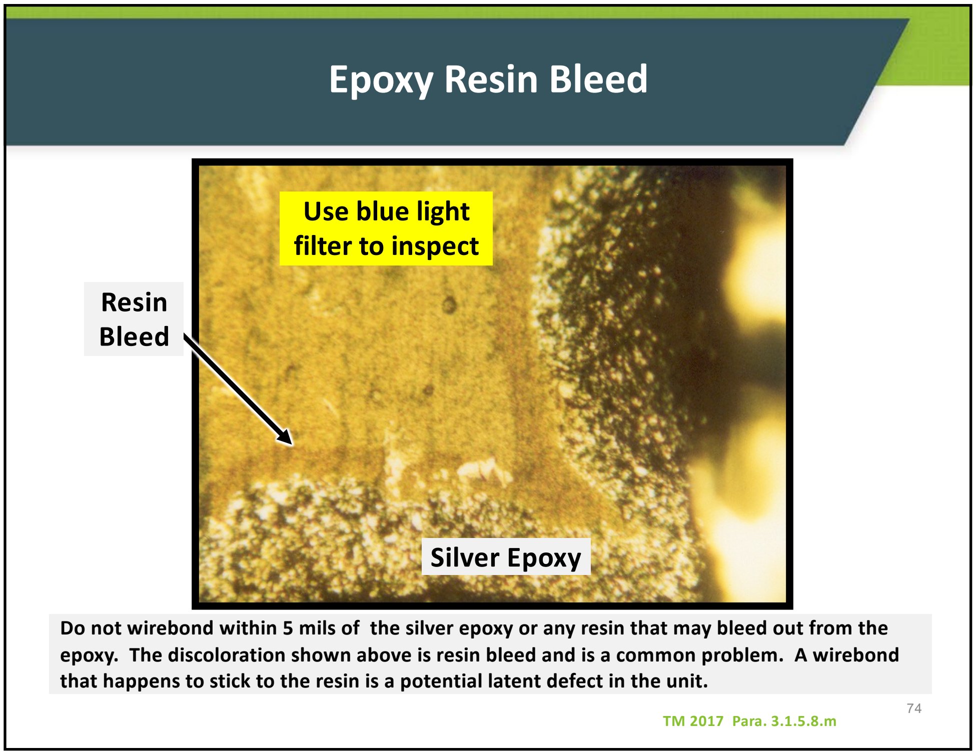
Excess Epoxy Fillet-Short

REJECT

Excess epoxy on the sidewall of this parallel plate chip capacitor. If the epoxy touches the top plate it will cause a short, and the device will not function. Ideally, the fillet should flow about halfway up the side, but at least one mil clearance to the top plate of the cap.

TM 2017 Para. 3.1.2.1.f

73



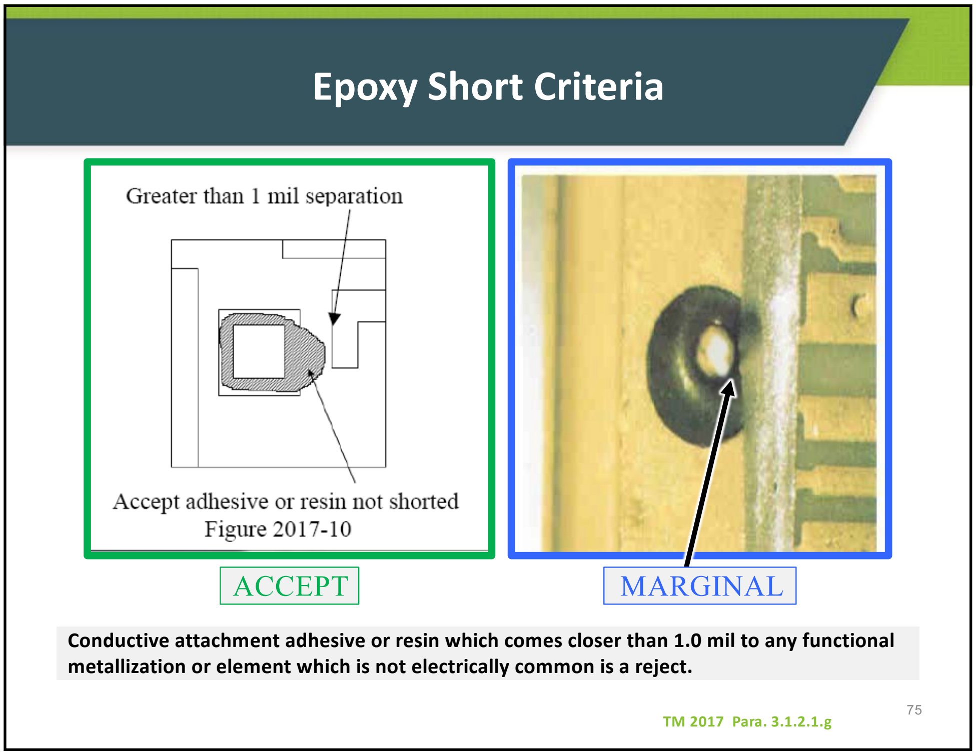
Epoxy Resin Bleed

Do not wirebond within 5 mils of the silver epoxy or any resin that may bleed out from the epoxy. The discoloration shown above is resin bleed and is a common problem. A wirebond that happens to stick to the resin is a potential latent defect in the unit.

TM 2017 Para. 3.1.5.8.m

74

Course Notes



Epoxy Short Criteria

Greater than 1 mil separation

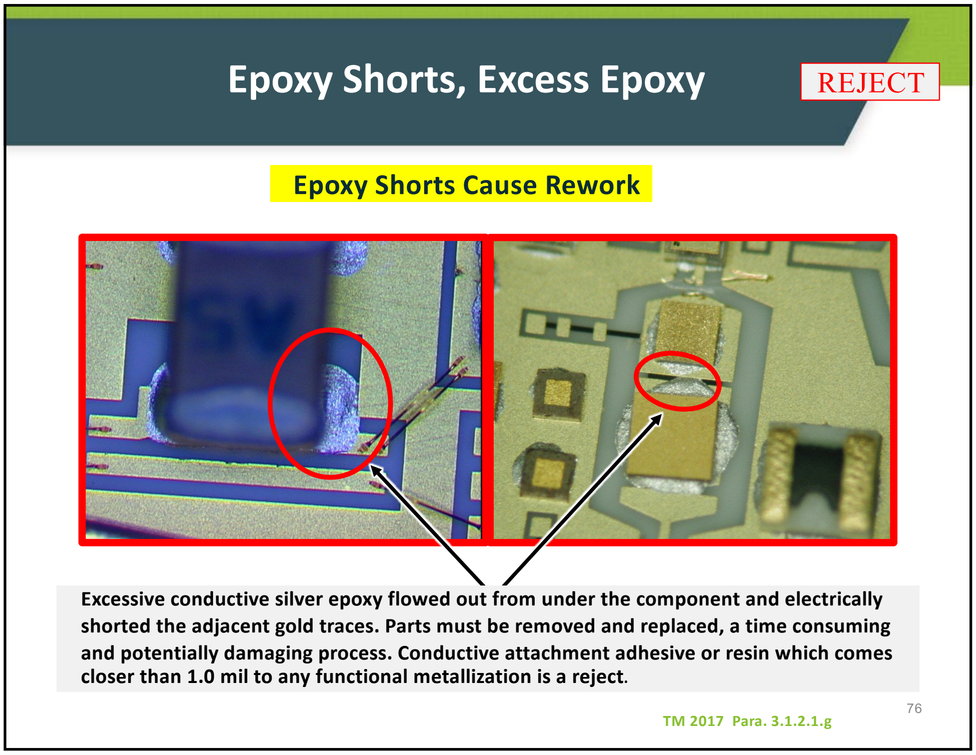
Accept adhesive or resin not shorted
Figure 2017-10

ACCEPT

MARGINAL

Conductive attachment adhesive or resin which comes closer than 1.0 mil to any functional metallization or element which is not electrically common is a reject.

TM 2017 Para. 3.1.2.1.g



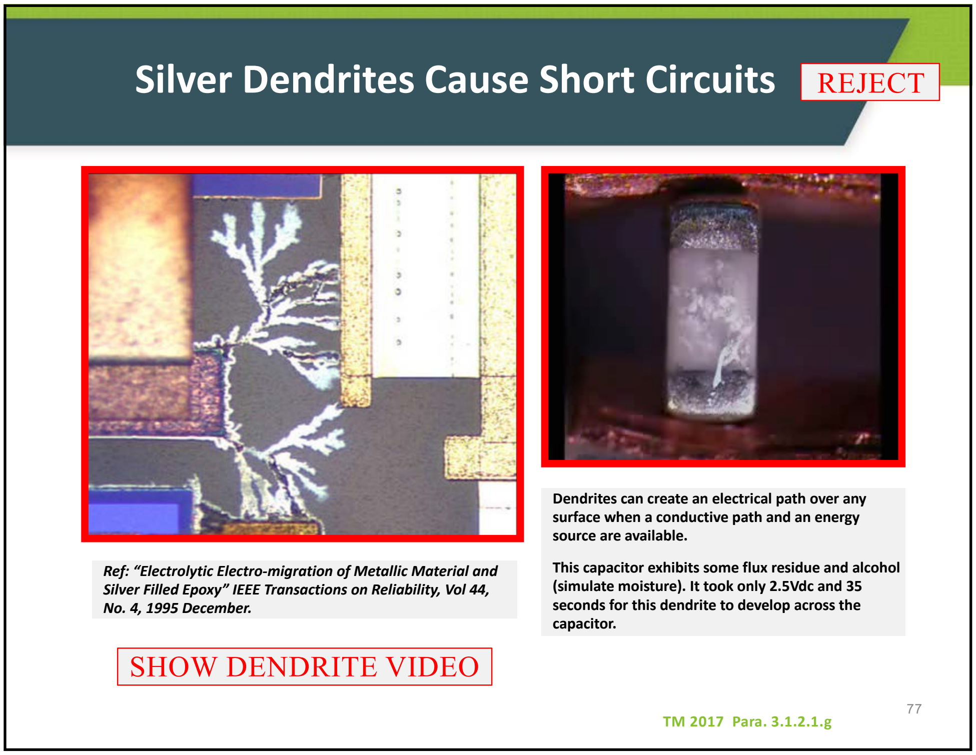
Epoxy Shorts, Excess Epoxy

REJECT

Epoxy Shorts Cause Rework

Excessive conductive silver epoxy flowed out from under the component and electrically shorted the adjacent gold traces. Parts must be removed and replaced, a time consuming and potentially damaging process. Conductive attachment adhesive or resin which comes closer than 1.0 mil to any functional metallization is a reject.

TM 2017 Para. 3.1.2.1.g



Silver Dendrites Cause Short Circuits

REJECT

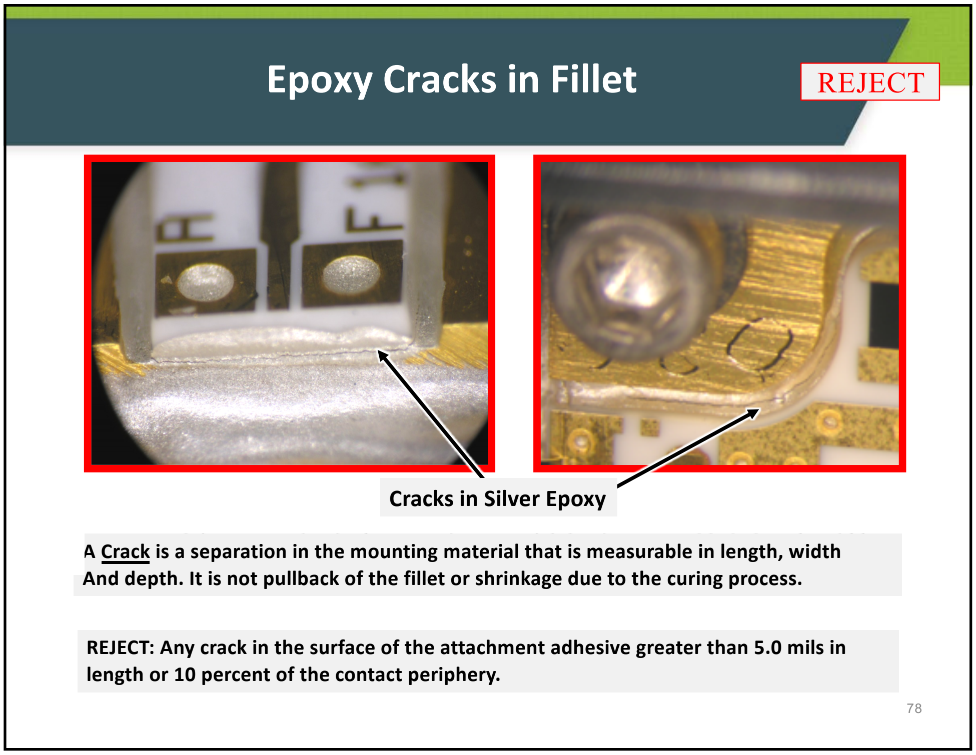
Ref: "Electrolytic Electro-migration of Metallic Material and Silver Filled Epoxy" IEEE Transactions on Reliability, Vol 44, No. 4, 1995 December.

Dendrites can create an electrical path over any surface when a conductive path and an energy source are available.

This capacitor exhibits some flux residue and alcohol (simulate moisture). It took only 2.5Vdc and 35 seconds for this dendrite to develop across the capacitor.

SHOW DENDRITE VIDEO

TM 2017 Para. 3.1.2.1.g



Epoxy Cracks in Fillet

REJECT

Cracks in Silver Epoxy

A Crack is a separation in the mounting material that is measurable in length, width And depth. It is not pullback of the fillet or shrinkage due to the curing process.

REJECT: Any crack in the surface of the attachment adhesive greater than 5.0 mils in length or 10 percent of the contact periphery.

Epoxy Cracks in Fillet

REJECT

Cracks in Silver Epoxy

A Crack is a separation in the mounting material that is measurable in length, width And depth. It is not pullback of the fillet or shrinkage due to the curing process.

REJECT: Any crack in the surface of the attachment adhesive greater than 5.0 mils in length or 10 percent of the contact periphery.

Silver Epoxy Fissures

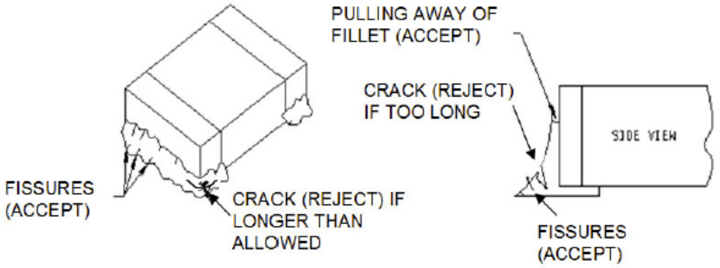
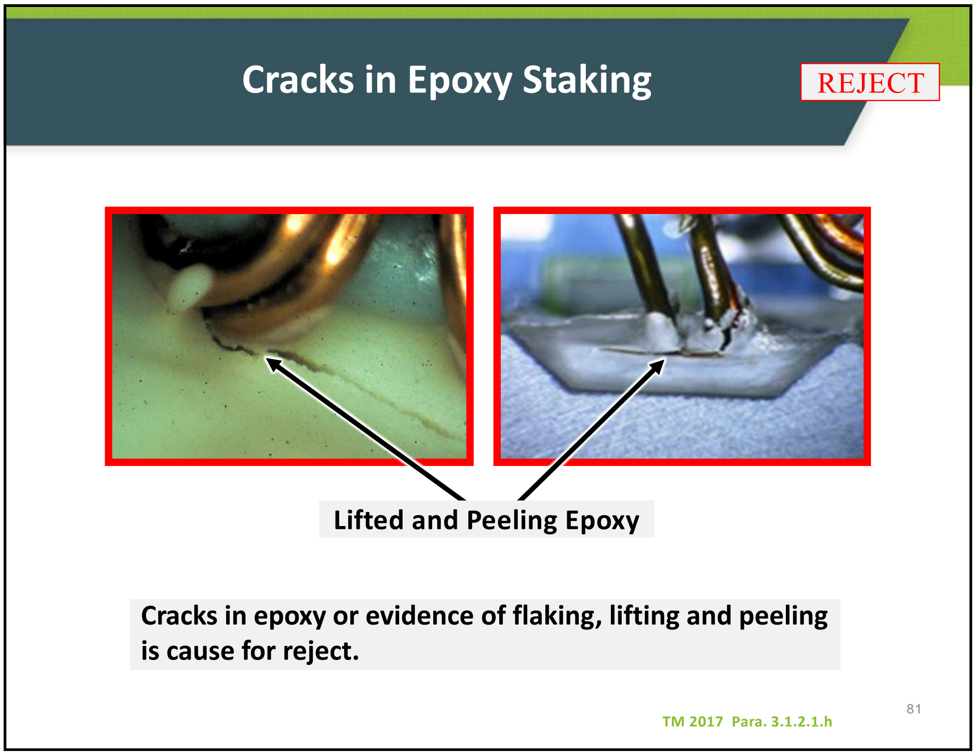


Figure 2017-11a.

Cracks in Silver Epoxy

There is a difference between a real crack and a fissure or surface anaomaly which often occur as the epoxy shrinks during the cure cycle.



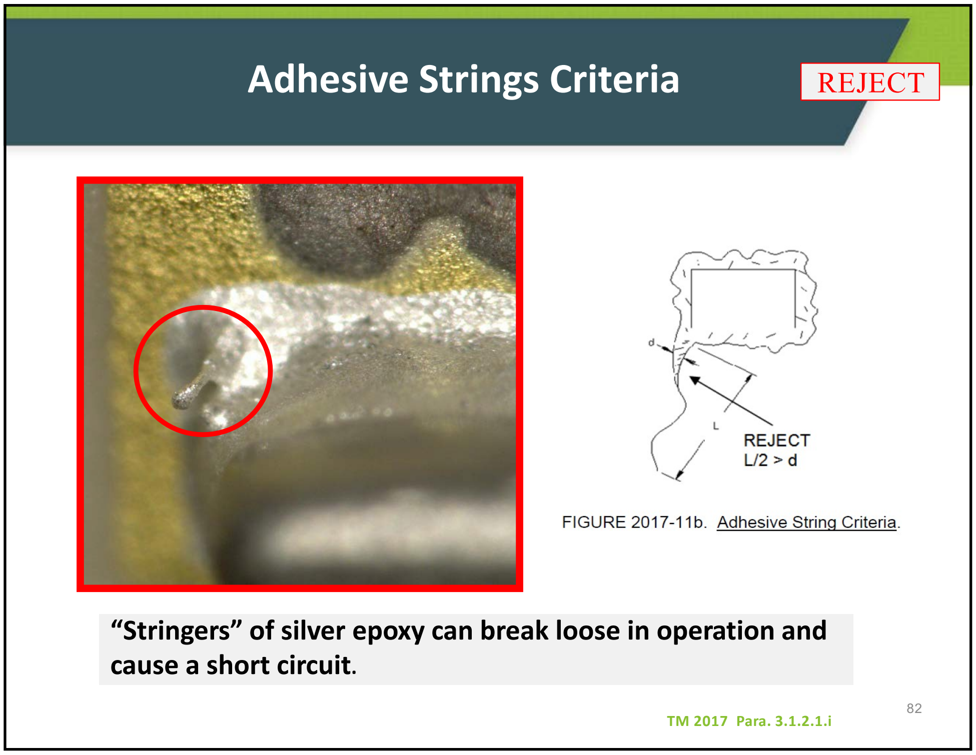
Cracks in Epoxy Staking

REJECT

Lifted and Peeling Epoxy

Cracks in epoxy or evidence of flaking, lifting and peeling is cause for reject.

TM 2017 Para. 3.1.2.1.h



Adhesive Strings Criteria

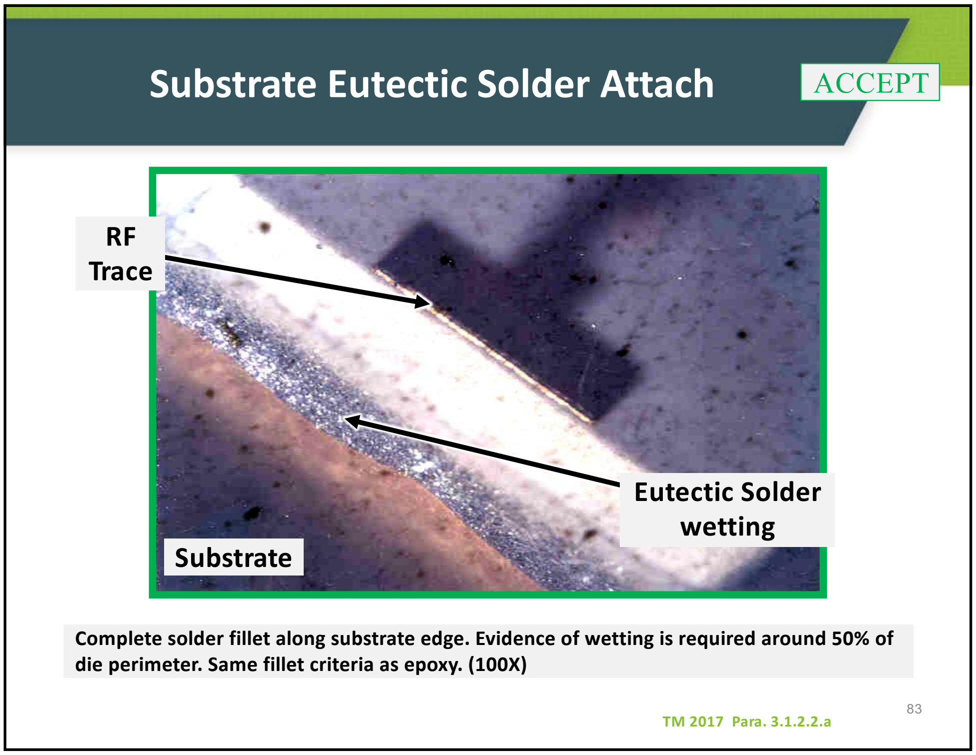
REJECT

FIGURE 2017-11b. Adhesive String Criteria.

“Stringers” of silver epoxy can break loose in operation and cause a short circuit.

TM 2017 Para. 3.1.2.1.i

Course Notes

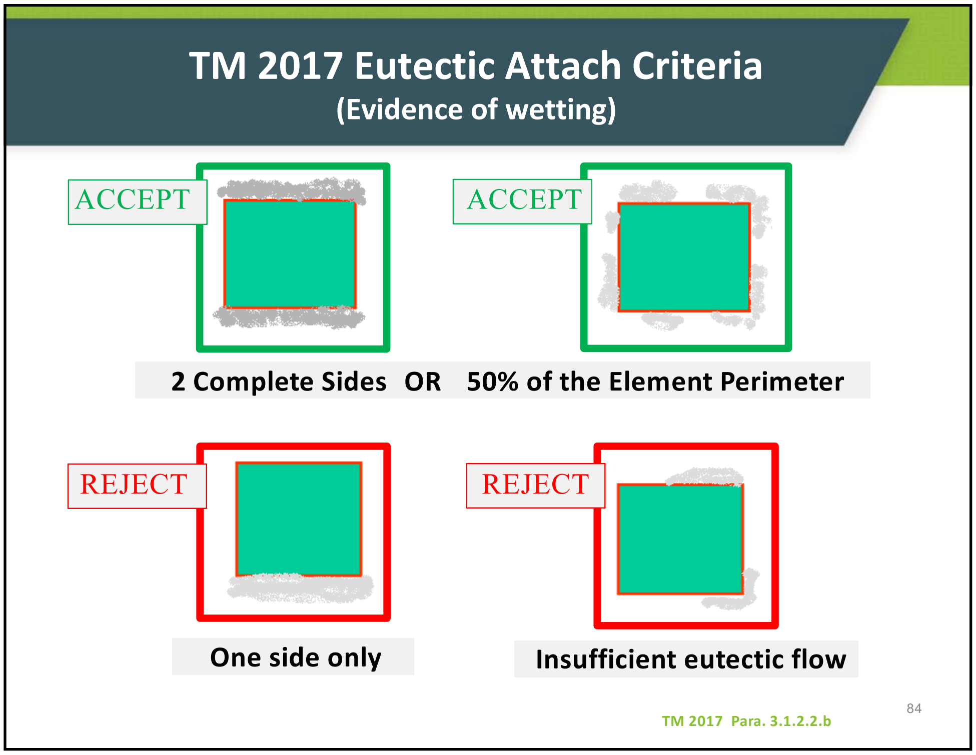


Substrate Eutectic Solder Attach

ACCEPT

Complete solder fillet along substrate edge. Evidence of wetting is required around 50% of die perimeter. Same fillet criteria as epoxy. (100X)

TM 2017 Para. 3.1.2.2.a



TM 2017 Eutectic Attach Criteria
(Evidence of wetting)

ACCEPT

ACCEPT

2 Complete Sides OR 50% of the Element Perimeter

REJECT

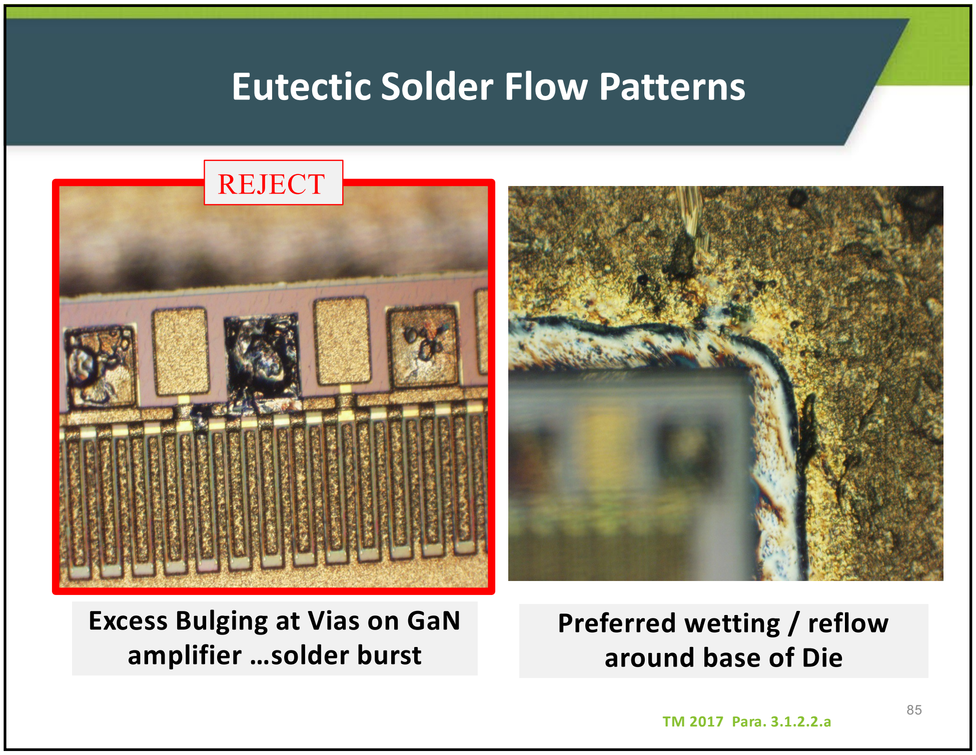
REJECT

One side only

Insufficient eutectic flow

TM 2017 Para. 3.1.2.2.b

Course Notes



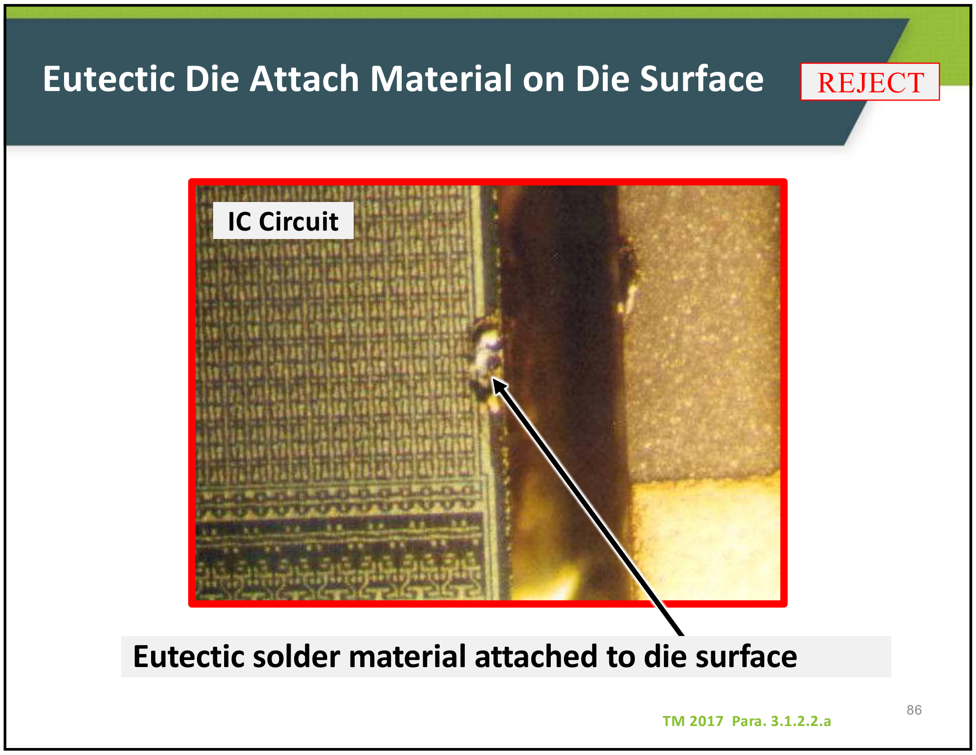
Eutectic Solder Flow Patterns

REJECT

Excess Bulging at Vias on GaN amplifier …solder burst

Preferred wetting / reflow around base of Die

TM 2017 Para. 3.1.2.2.a



Eutectic Die Attach Material on Die Surface

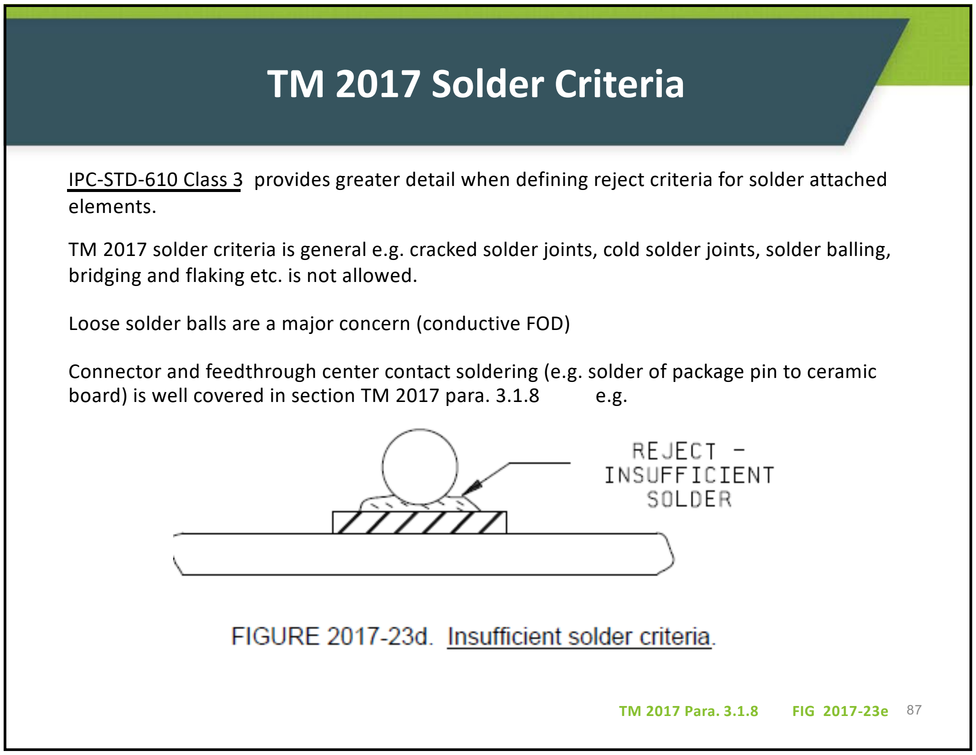
REJECT

IC Circuit

Eutectic solder material attached to die surface

TM 2017 Para. 3.1.2.2.a

Course Notes



TM 2017 Solder Criteria

IPC-STD-610 Class 3 provides greater detail when defining reject criteria for solder attached elements.

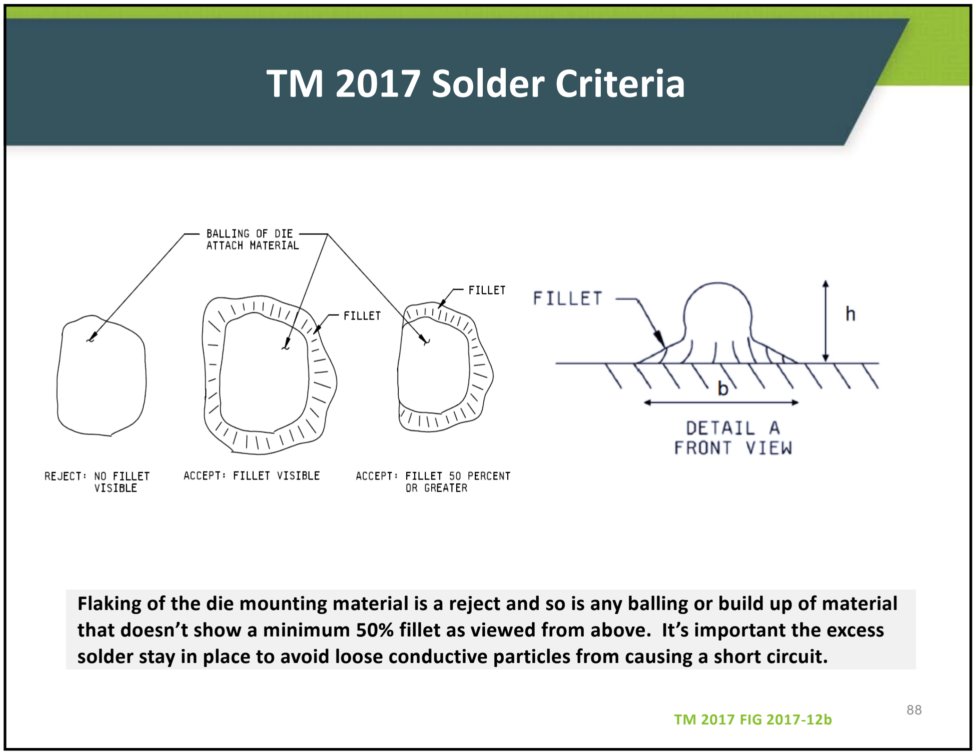
TM 2017 solder criteria is general e.g. cracked solder joints, cold solder joints, solder balling, bridging and flaking etc. is not allowed.

Loose solder balls are a major concern (conductive FOD)

Connector and feedthrough center contact soldering (e.g. solder of package pin to ceramic board) is well covered in section TM 2017 para. 3.1.8 e.g.

FIGURE 2017-23d. Insufficient solder criteria.

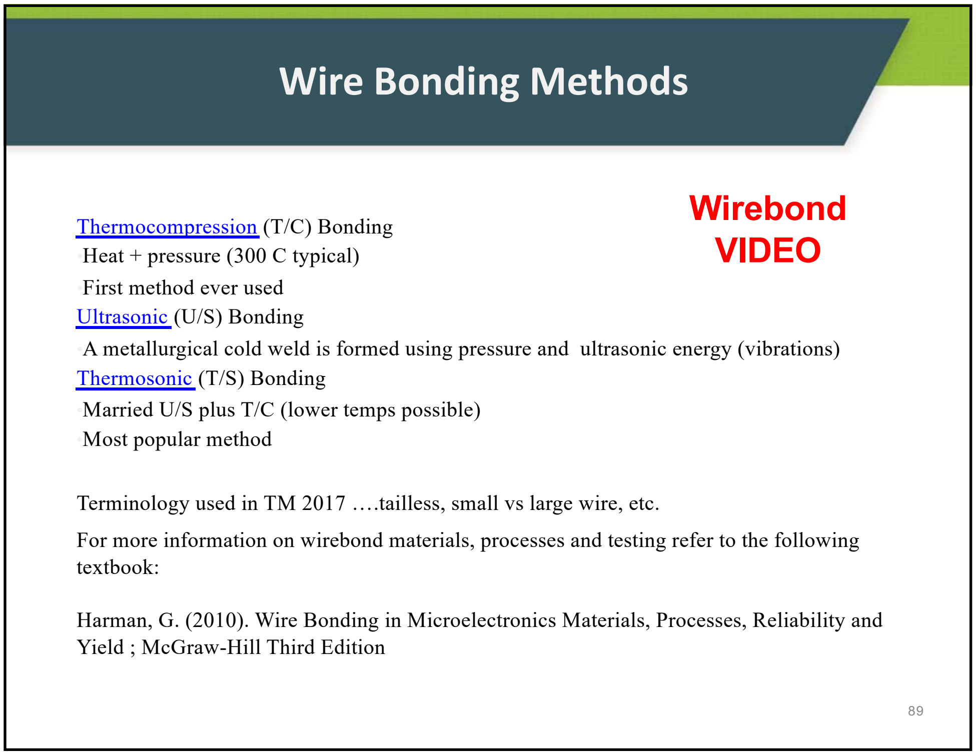
TM 2017 Para. 3.1.8 FIG 2017-23e



TM 2017 Solder Criteria

Flaking of the die mounting material is a reject and so is any balling or build up of material that doesn't show a minimum 50% fillet as viewed from above. It's important the excess solder stay in place to avoid loose conductive particles from causing a short circuit.

TM 2017 FIG 2017-12b



Wire Bonding Methods

Wirebond VIDEO

Thermocompression (T/C) Bonding
- Heat + pressure (300 C typical)
- First method ever used

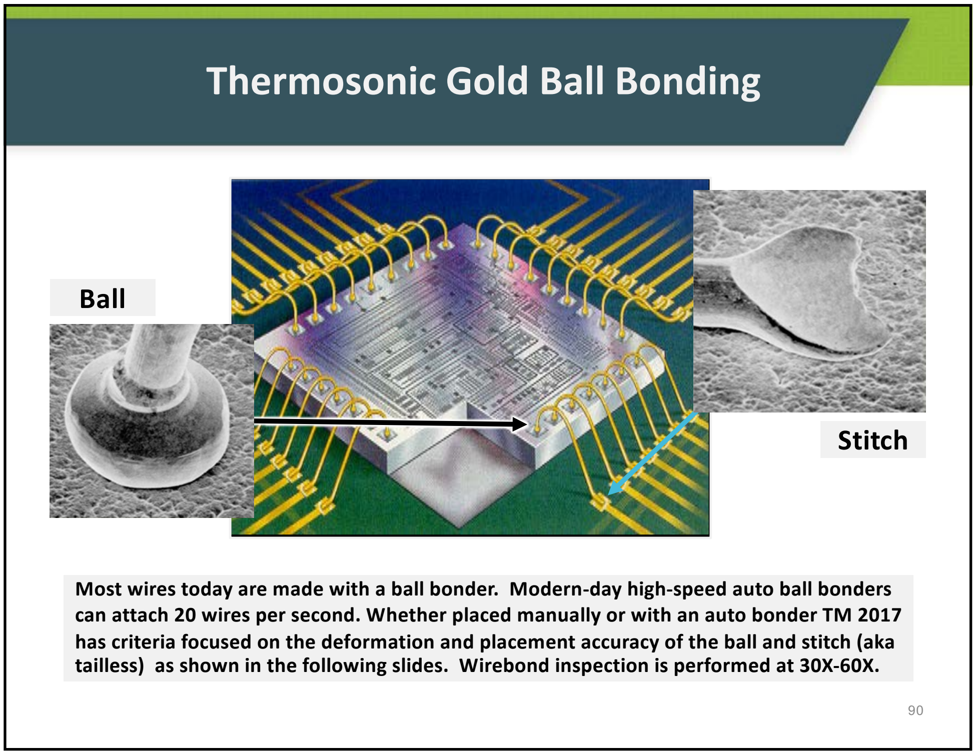
Ultrasonic (U/S) Bonding
- A metallurgical cold weld is formed using pressure and ultrasonic energy (vibrations)

Thermosonic (T/S) Bonding
- Married U/S plus T/C (lower temps possible)
- Most popular method

Terminology used in TM 2017 ….tailless, small vs large wire, etc.

For more information on wirebond materials, processes and testing refer to the following textbook:

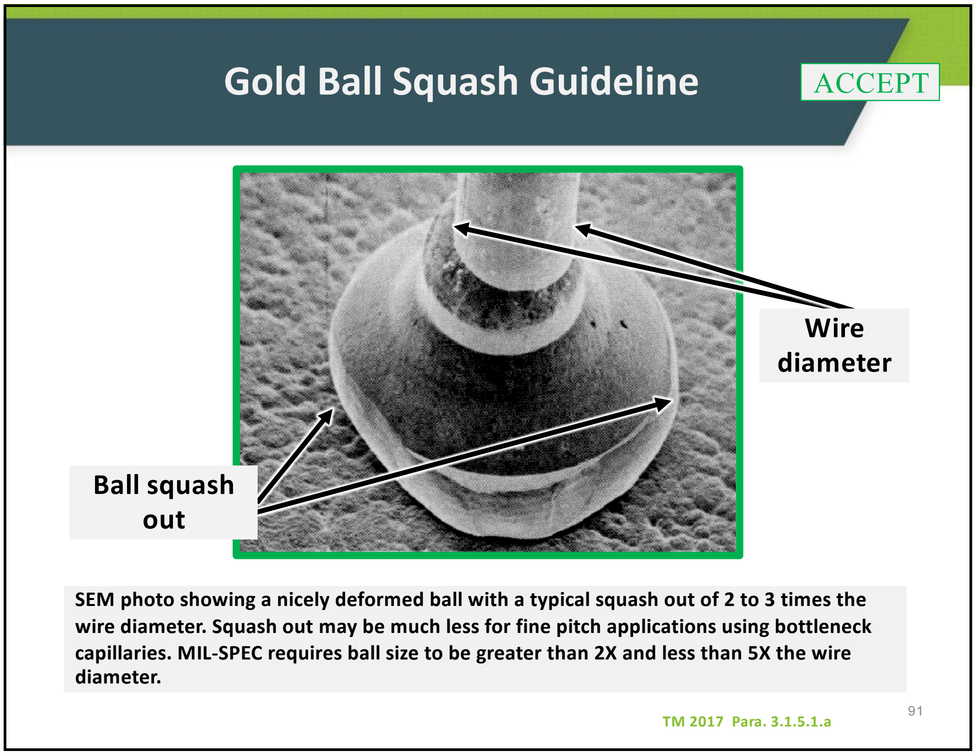
Harman, G. (2010). Wire Bonding in Microelectronics Materials, Processes, Reliability and Yield ; McGraw-Hill Third Edition



Thermosonic Gold Ball Bonding

Most wires today are made with a ball bonder. Modern-day high-speed auto ball bonders can attach 20 wires per second. Whether placed manually or with an auto bonder TM 2017 has criteria focused on the deformation and placement accuracy of the ball and stitch (aka tailless) as shown in the following slides. Wirebond inspection is performed at 30X-60X.

Course Notes

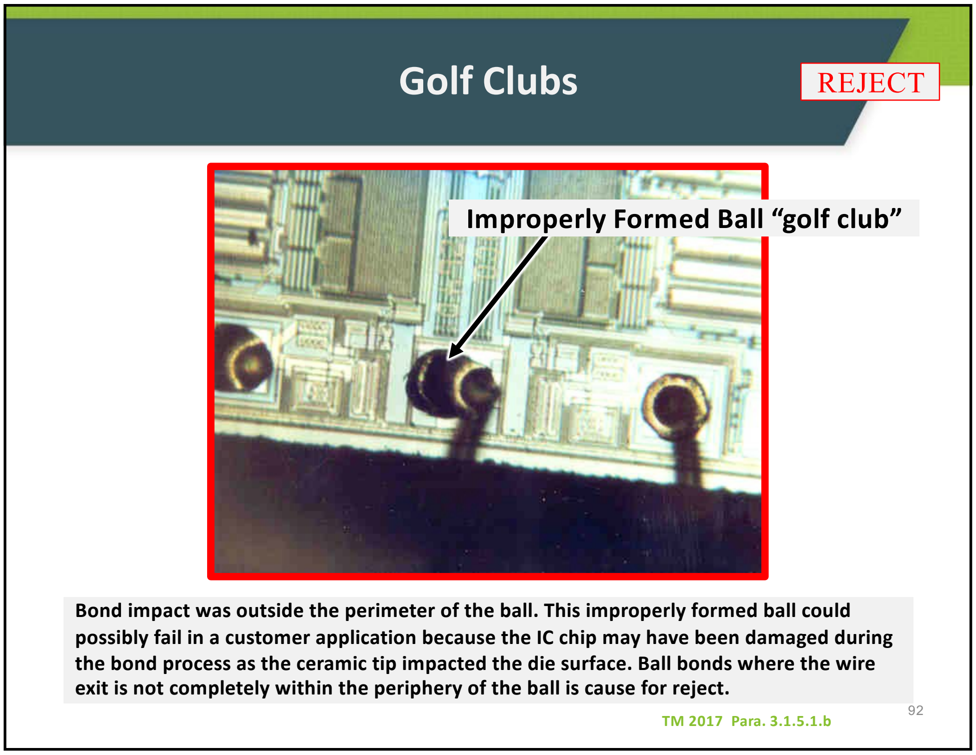


Gold Ball Squash Guideline

ACCEPT

SEM photo showing a nicely deformed ball with a typical squash out of 2 to 3 times the wire diameter. Squash out may be much less for fine pitch applications using bottleneck capillaries. MIL-SPEC requires ball size to be greater than 2X and less than 5X the wire diameter.

TM 2017 Para. 3.1.5.1.a



Golf Clubs

REJECT

Bond impact was outside the perimeter of the ball. This improperly formed ball could possibly fail in a customer application because the IC chip may have been damaged during the bond process as the ceramic tip impacted the die surface. Ball bonds where the wire exit is not completely within the periphery of the ball is cause for reject.

TM 2017 Para. 3.1.5.1.b

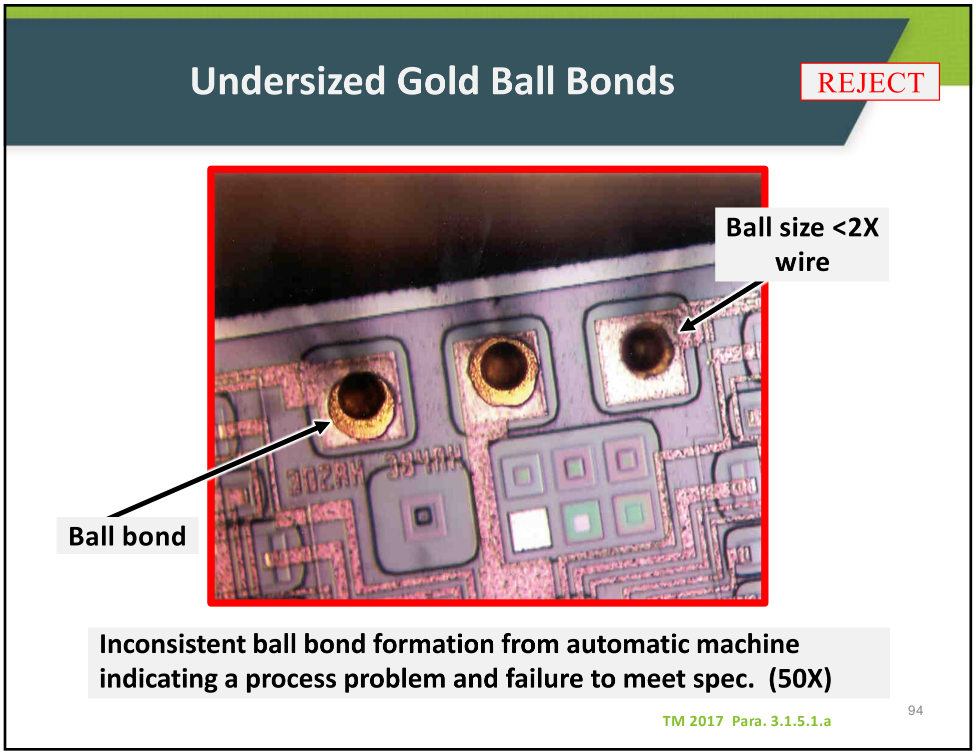
Course Notes

Golf Clubs Gold Ball Bonds

MARGINAL

SEM photo showing "golf-clubbing" of a ball bond, possibly the result of excessive tail length, improper wire tension or incorrect electrode to wire gap setting. Bonds like this indicate the process is slipping out of control and the process/equipment/material system must be adjusted.

TM 2017 Para. 3.1.5.1.a



Undersized Gold Ball Bonds

REJECT

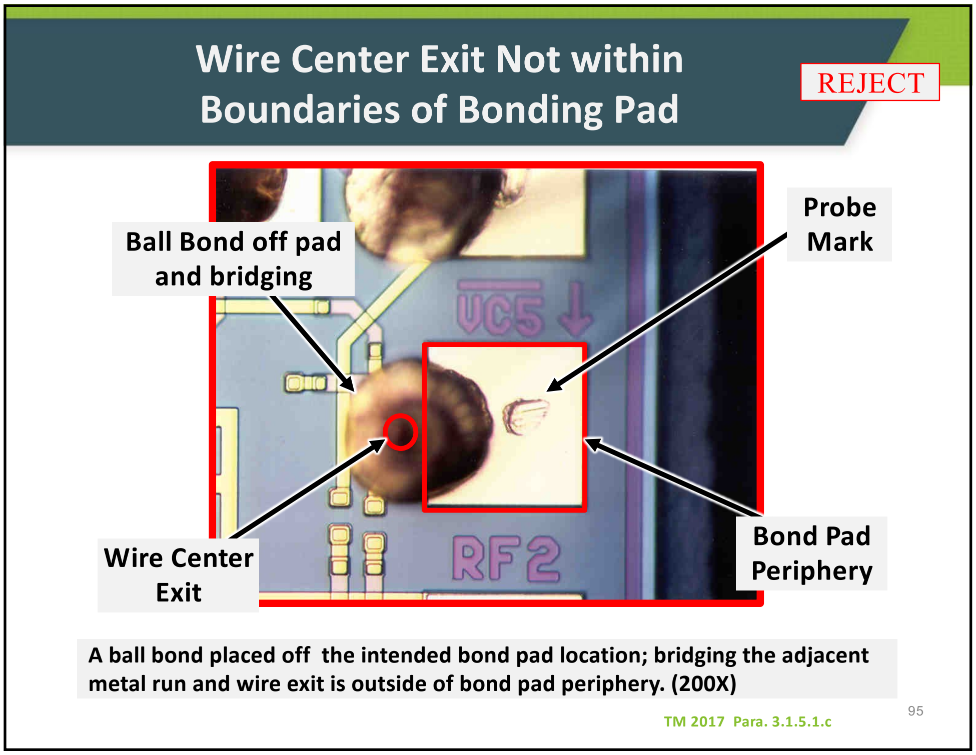
Ball size <2X wire

Ball bond

Inconsistent ball bond formation from automatic machine indicating a process problem and failure to meet spec. (50X)

TM 2017 Para. 3.1.5.1.a

Course Notes



Wire Center Exit Not within Boundaries of Bonding Pad

REJECT

Ball Bond off pad and bridging

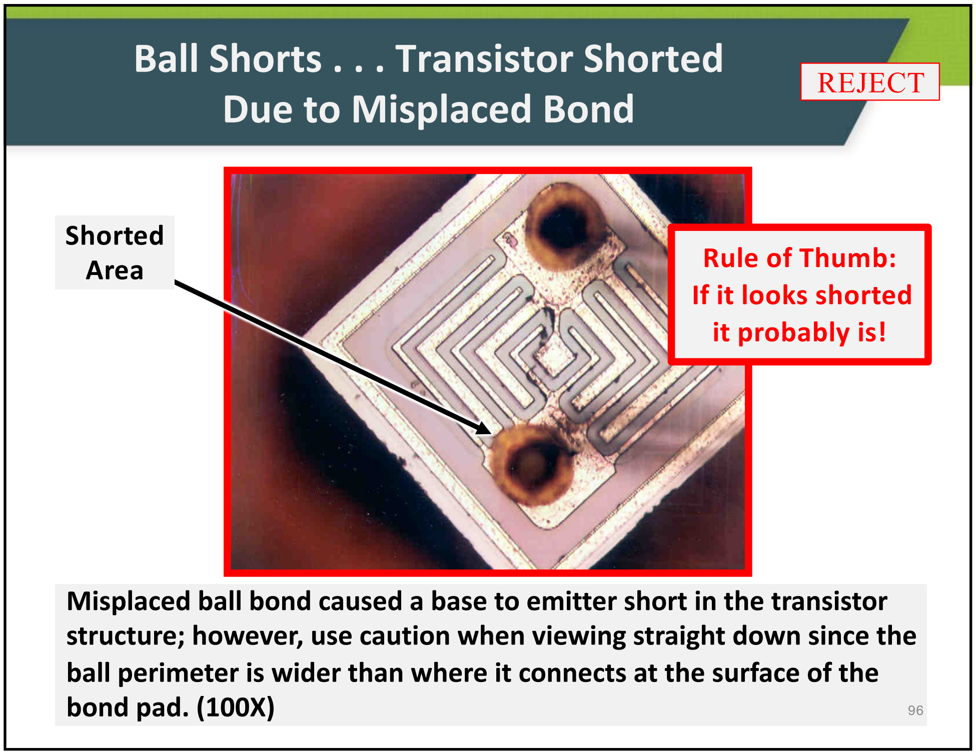
Probe Mark

Wire Center Exit

Bond Pad Periphery

A ball bond placed off the intended bond pad location; bridging the adjacent metal run and wire exit is outside of bond pad periphery. (200X)

TM 2017 Para. 3.1.5.1.c



Ball Shorts . . . Transistor Shorted Due to Misplaced Bond

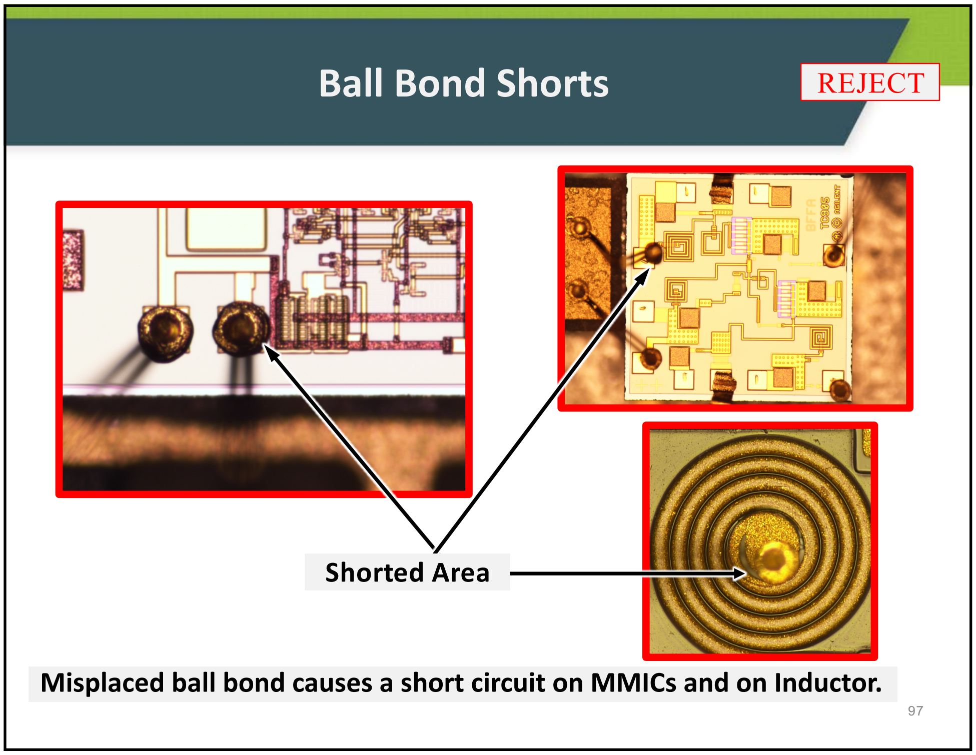
REJECT

Shorted Area

Rule of Thumb:
If it looks shorted
it probably is!

Misplaced ball bond caused a base to emitter short in the transistor structure; however, use caution when viewing straight down since the ball perimeter is wider than where it connects at the surface of the bond pad. (100X)

Course Notes

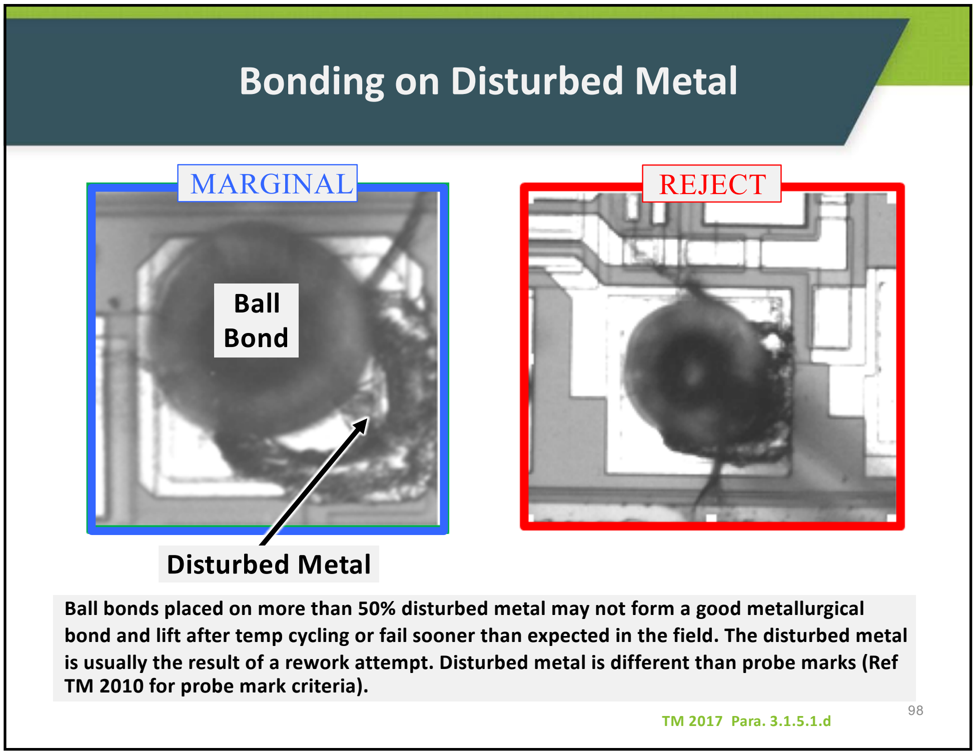


Ball Bond Shorts

REJECT

Shorted Area

Misplaced ball bond causes a short circuit on MMICs and on Inductor.



Bonding on Disturbed Metal

MARGINAL

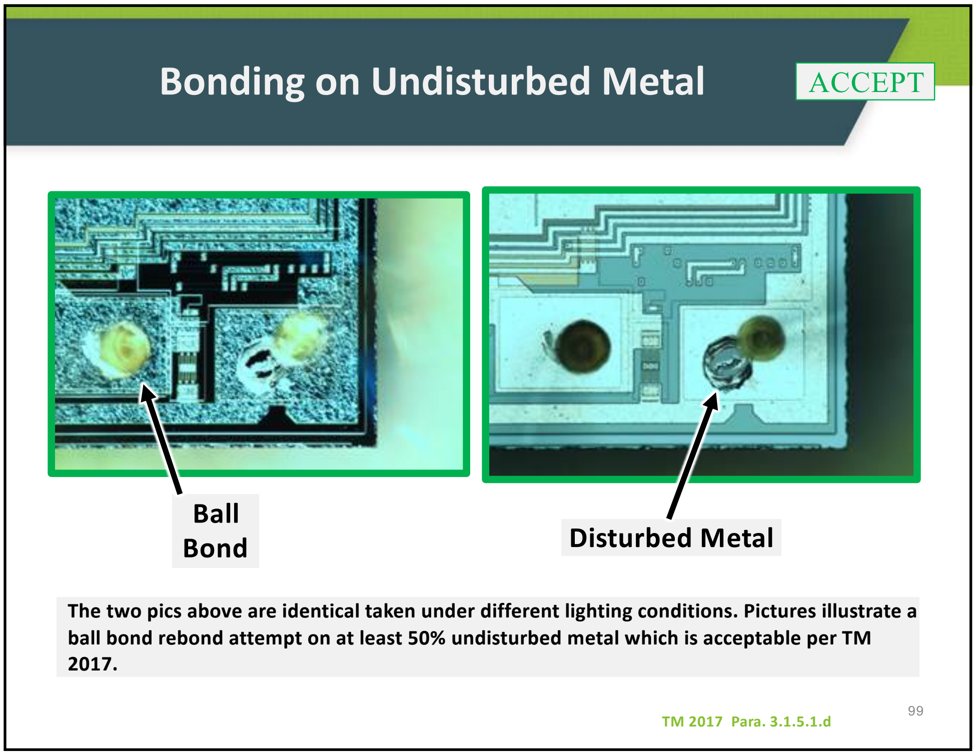
Ball Bond

Disturbed Metal

REJECT

Ball bonds placed on more than 50% disturbed metal may not form a good metallurgical bond and lift after temp cycling or fail sooner than expected in the field. The disturbed metal is usually the result of a rework attempt. Disturbed metal is different than probe marks (Ref TM 2010 for probe mark criteria).

TM 2017 Para. 3.1.5.1.d



Bonding on Undisturbed Metal

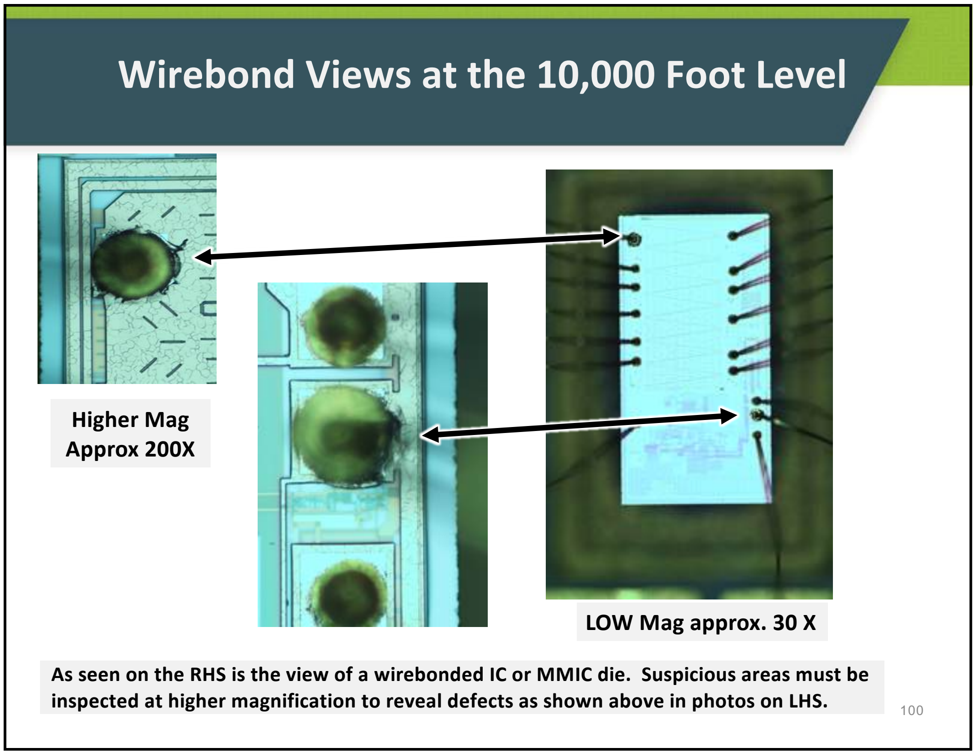
ACCEPT

Ball Bond

Disturbed Metal

The two pics above are identical taken under different lighting conditions. Pictures illustrate a ball bond rebond attempt on at least 50% undisturbed metal which is acceptable per TM 2017.

TM 2017 Para. 3.1.5.1.d

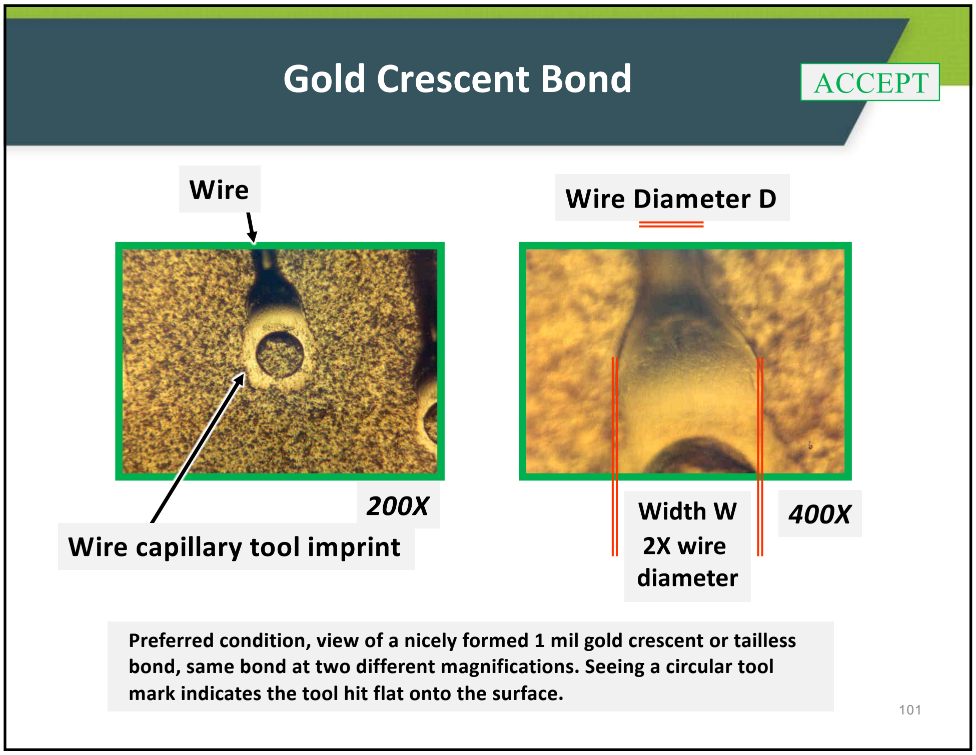


Wirebond Views at the 10,000 Foot Level

Higher Mag Approx 200X

LOW Mag approx. 30 X

As seen on the RHS is the view of a wirebonded IC or MMIC die. Suspicious areas must be inspected at higher magnification to reveal defects as shown above in photos on LHS.



Gold Crescent Bond

ACCEPT

Wire

Wire Diameter D

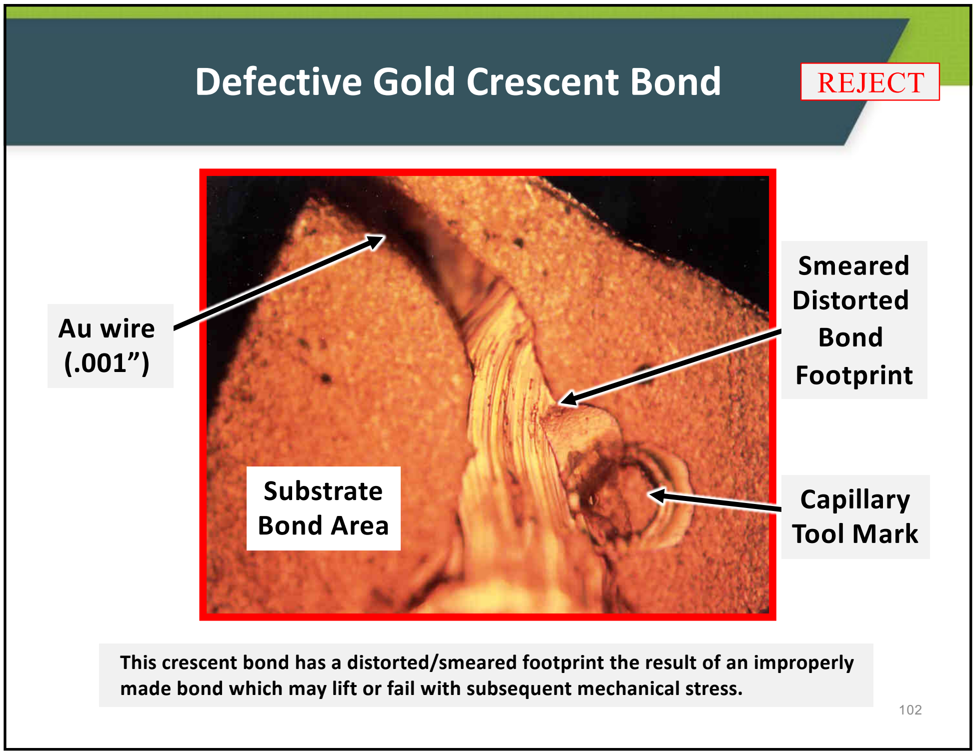
200X

Wire capillary tool imprint

Width W
2X wire
diameter

400X

Preferred condition, view of a nicely formed 1 mil gold crescent or tailless bond, same bond at two different magnifications. Seeing a circular tool mark indicates the tool hit flat onto the surface.



Defective Gold Crescent Bond

REJECT

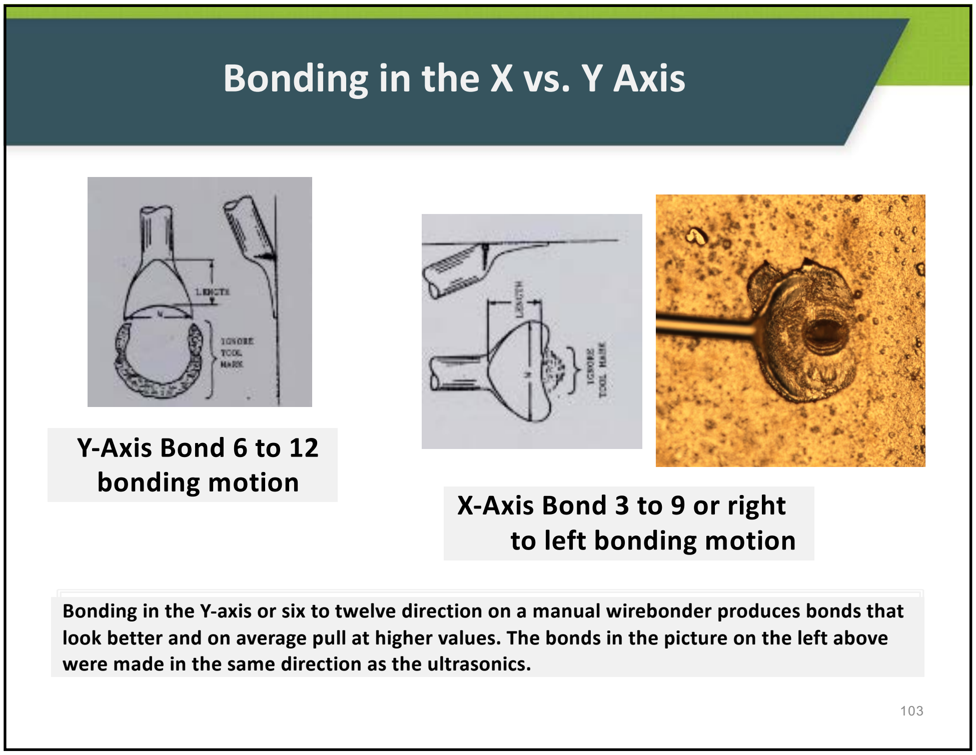
Au wire
(.001”)

Smeared
Distorted
Bond
Footprint

Substrate
Bond Area

Capillary
Tool Mark

This crescent bond has a distorted/smeared footprint the result of an improperly made bond which may lift or fail with subsequent mechanical stress.

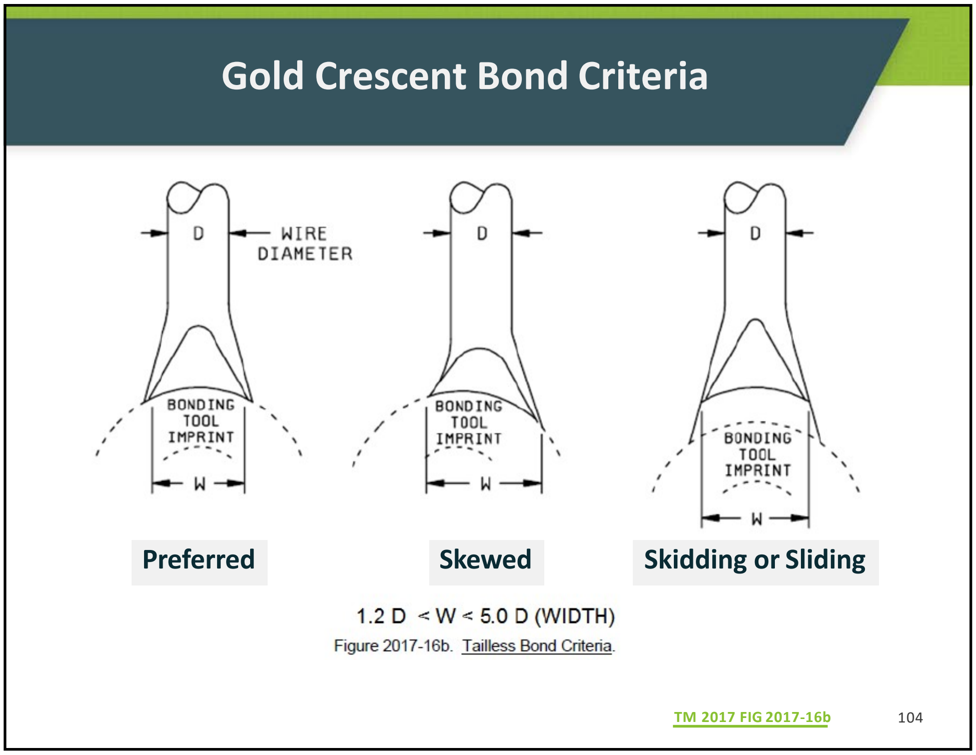


Bonding in the X vs. Y Axis

Y-Axis Bond 6 to 12 bonding motion

X-Axis Bond 3 to 9 or right to left bonding motion

Bonding in the Y-axis or six to twelve direction on a manual wirebonder produces bonds that look better and on average pull at higher values. The bonds in the picture on the left above were made in the same direction as the ultrasonics.



Gold Crescent Bond Criteria

Preferred

Skewed

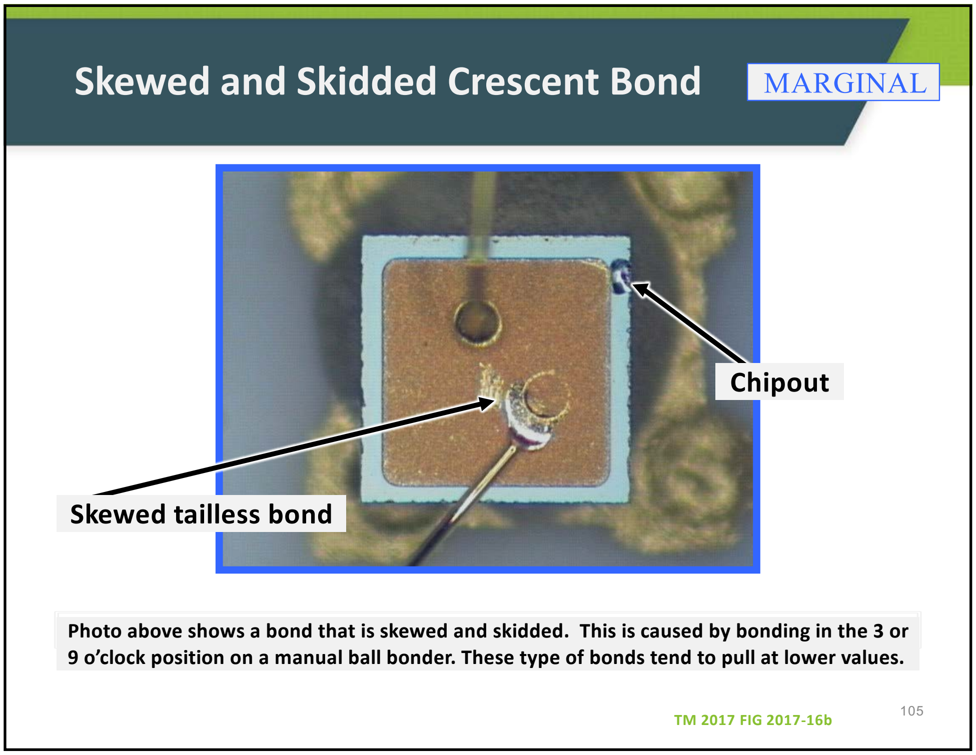
Skidding or Sliding

1.2 D < W < 5.0 D (WIDTH)

Figure 2017-16b. Tailless Bond Criteria.

TM 2017 FIG 2017-16b

Course Notes

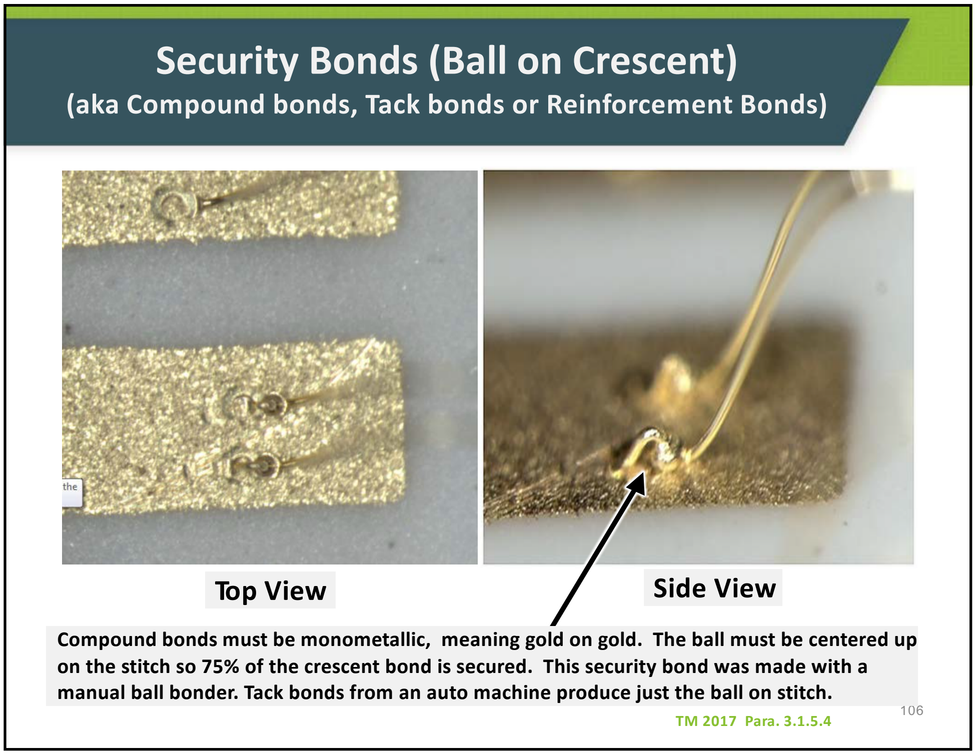


Skewed and Skidded Crescent Bond

MARGINAL

Photo above shows a bond that is skewed and skidded. This is caused by bonding in the 3 or 9 o'clock position on a manual ball bonder. These type of bonds tend to pull at lower values.

TM 2017 FIG 2017-16b



Security Bonds (Ball on Crescent)
(aka Compound bonds, Tack bonds or Reinforcement Bonds)

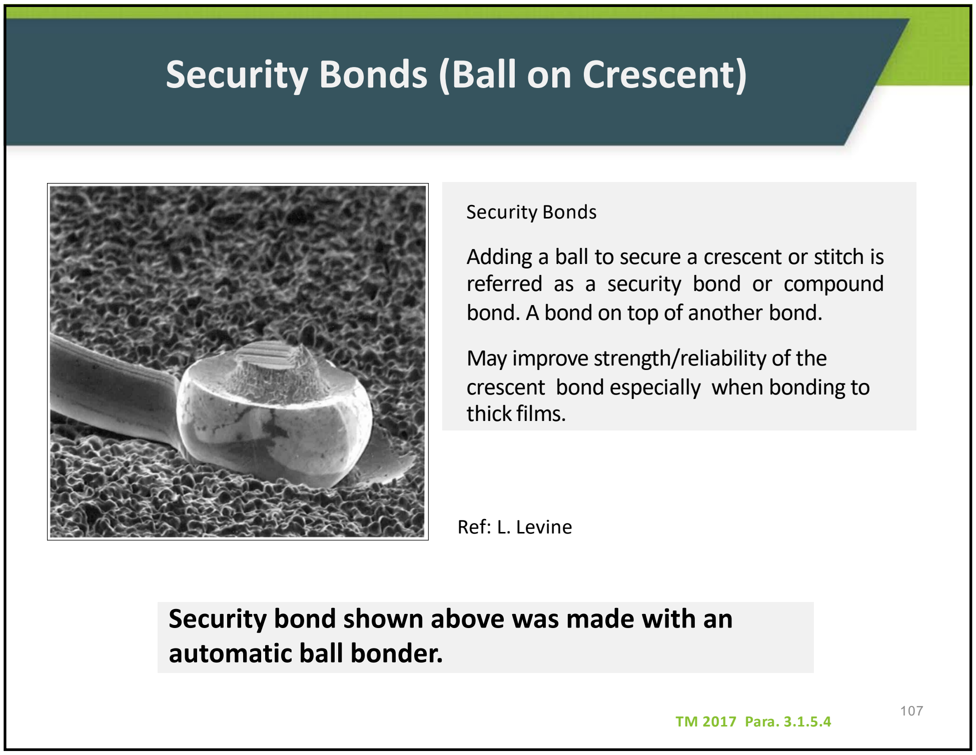
Top View

Side View

Compound bonds must be monometallic, meaning gold on gold. The ball must be centered up on the stitch so 75% of the crescent bond is secured. This security bond was made with a manual ball bonder. Tack bonds from an auto machine produce just the ball on stitch.

TM 2017 Para. 3.1.5.4

Course Notes



Security Bonds (Ball on Crescent)

Security Bonds

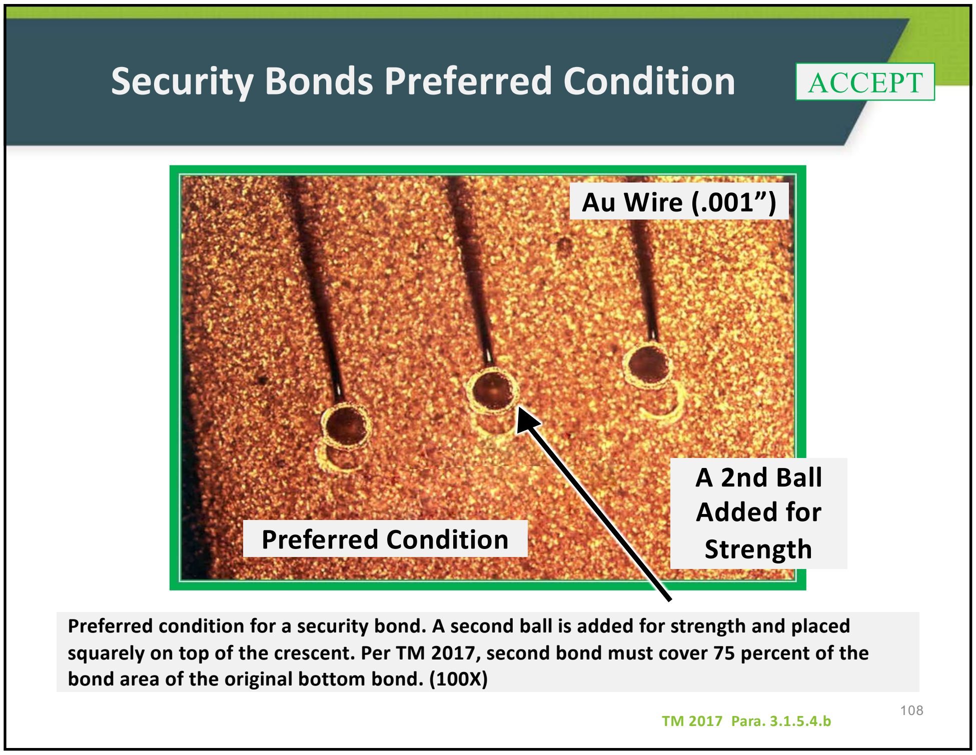
Adding a ball to secure a crescent or stitch is referred as a security bond or compound bond. A bond on top of another bond.

May improve strength/reliability of the crescent bond especially when bonding to thick films.

Ref: L. Levine

Security bond shown above was made with an automatic ball bonder.

TM 2017 Para. 3.1.5.4



Security Bonds Preferred Condition

ACCEPT

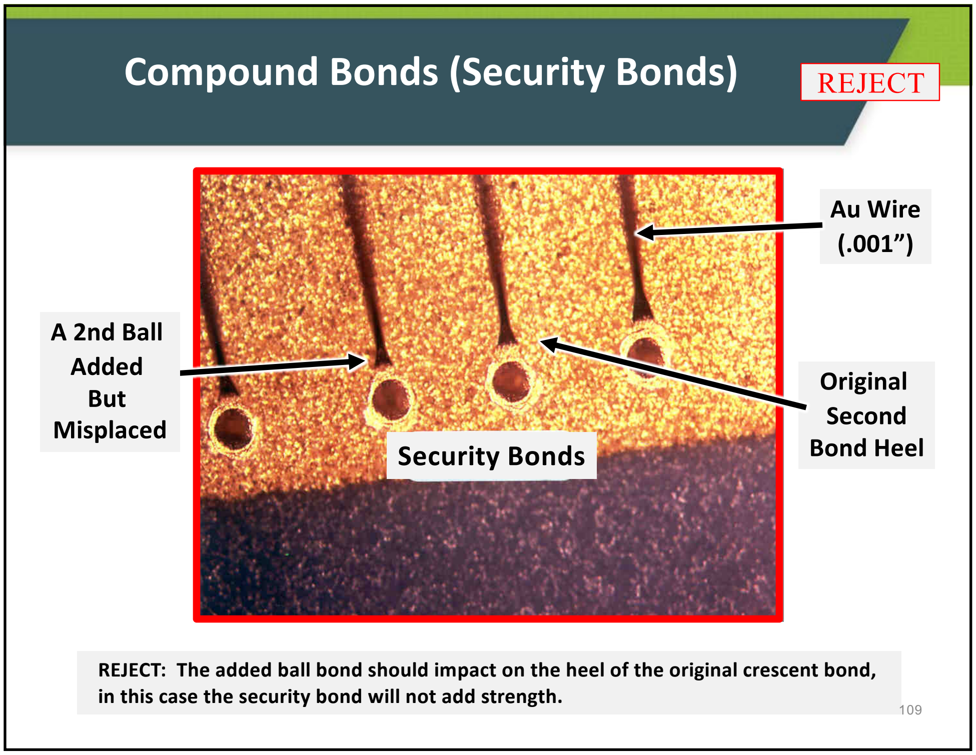
Au Wire (.001")

A 2nd Ball Added for Strength

Preferred Condition

Preferred condition for a security bond. A second ball is added for strength and placed squarely on top of the crescent. Per TM 2017, second bond must cover 75 percent of the bond area of the original bottom bond. (100X)

TM 2017 Para. 3.1.5.4.b



Compound Bonds (Security Bonds)

REJECT

Au Wire (.001")

A 2nd Ball Added But Misplaced

Original Second Bond Heel

Security Bonds

REJECT: The added ball bond should impact on the heel of the original crescent bond, in this case the security bond will not add strength.

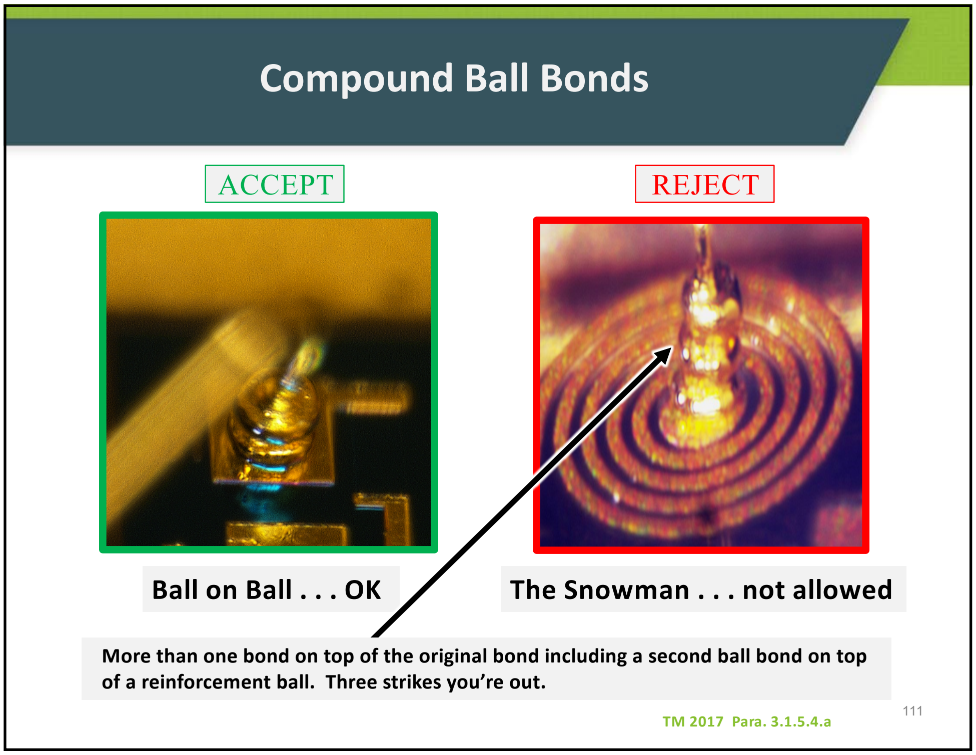
Security Bonds . . . The Good , the Bad and the Ugly!

The Good

The Bad

THE UGLY!

Security bonds need to be at least 75% centered over the crescent and not on the wire.



Compound Ball Bonds

ACCEPT

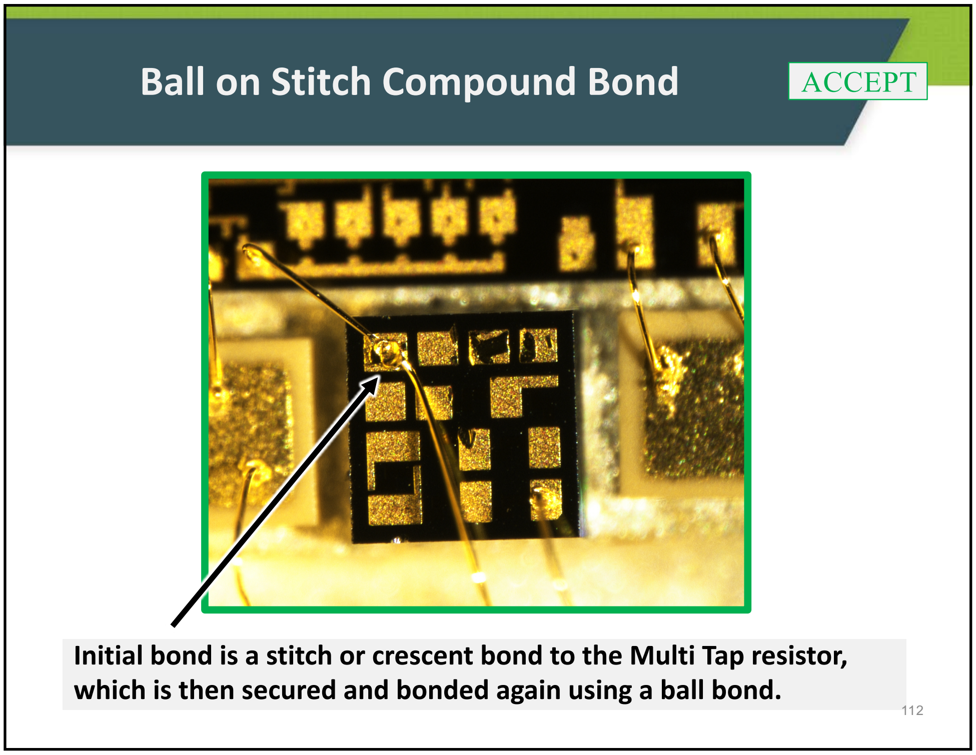
REJECT

Ball on Ball . . . OK

The Snowman . . . not allowed

More than one bond on top of the original bond including a second ball bond on top of a reinforcement ball. Three strikes you're out.

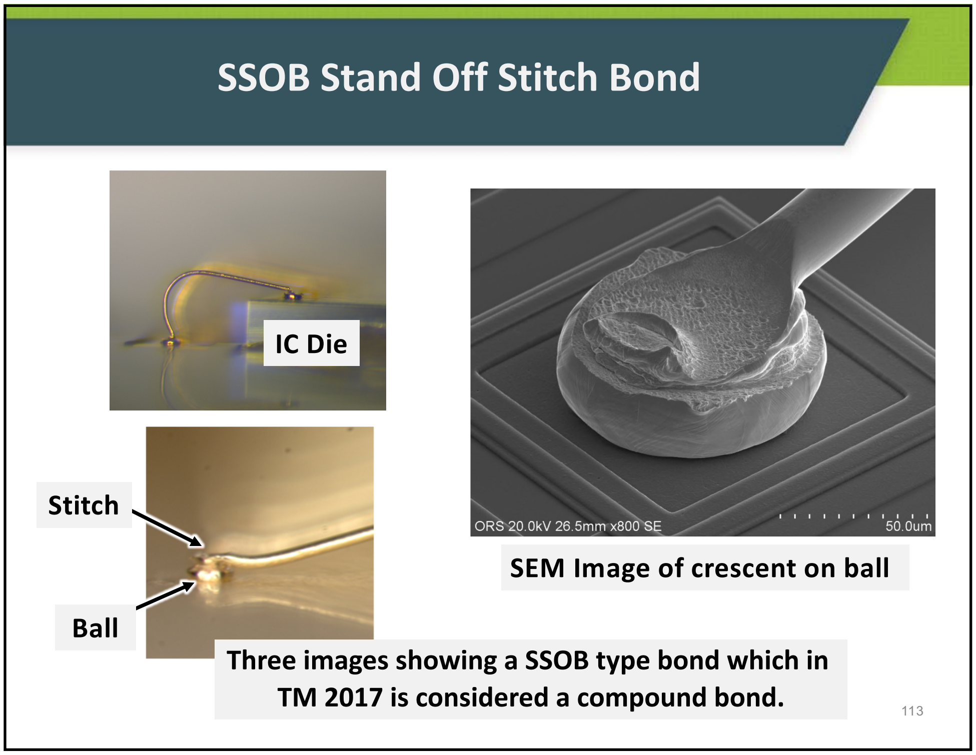
TM 2017 Para. 3.1.5.4.a



Ball on Stitch Compound Bond

ACCEPT

Initial bond is a stitch or crescent bond to the Multi Tap resistor, which is then secured and bonded again using a ball bond.



SSOB Stand Off Stitch Bond

SEM Image of crescent on ball

Three images showing a SSOB type bond which in TM 2017 is considered a compound bond.

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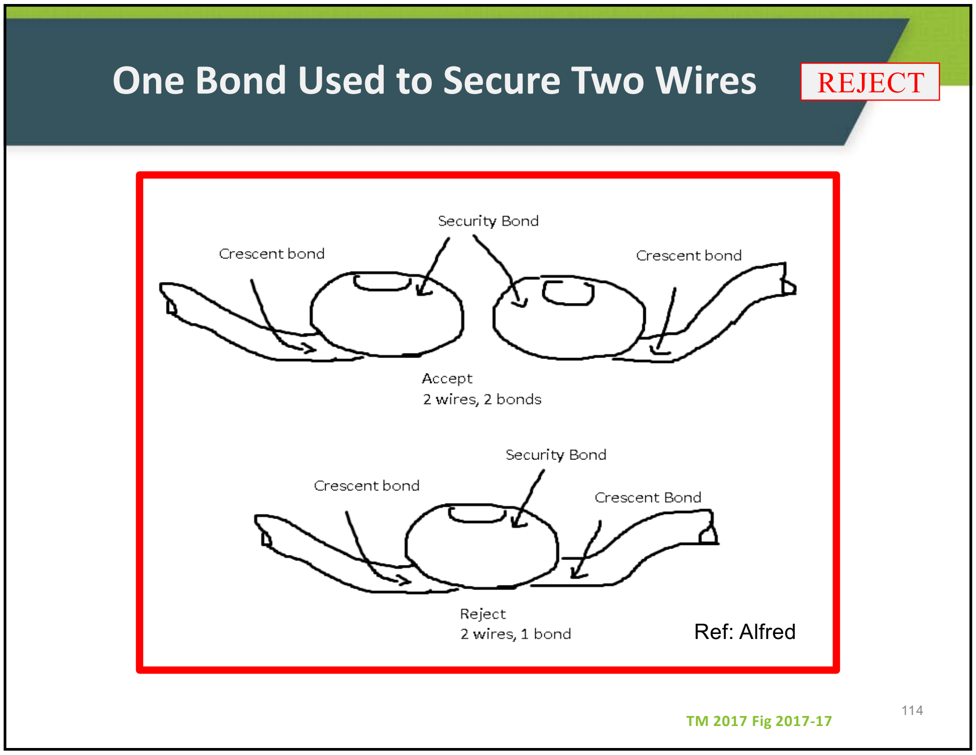

One Bond Used to Secure Two Wires

REJECT

Ref: Alfred

TM 2017 Fig 2017-17

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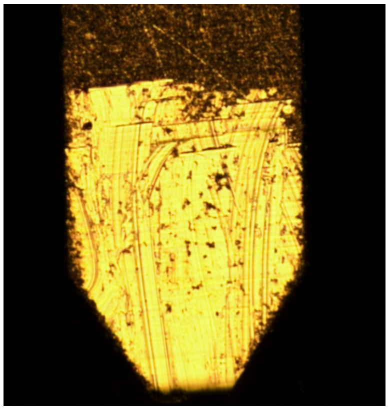
General Wirebond REJECT Criteria

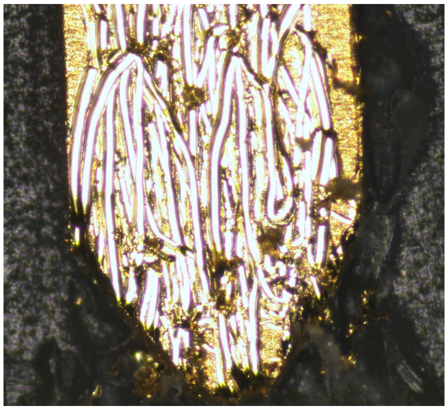
- Bonds on the die where less than 50 percent of the bond is within the unglassivated bonding site.
- Bonds on the package post or substrate that are not completely within the bonding site.
- An absence of a visible line of separation between non-electrically common bonds.
- An absence of a visible line of separation between a bond and non-electrically common metallization. This criteria applies to both glassivated and unglassivated metallization.

TM 2017 Para. 3.1.5.8

Burnishing for Wirebond Purposes



ACCEPTABLE

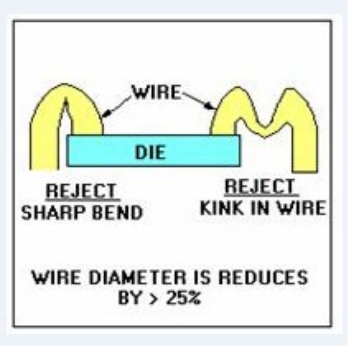


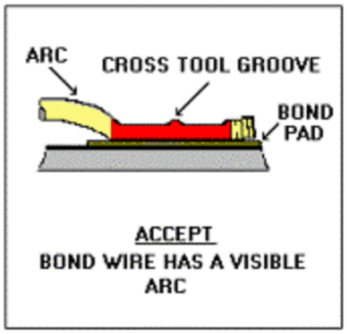
UNACCEPTABLE

In some cases a thick film trace on ceramic substrate or a package post needs to be cleaned using a tool to scrape away surface contaminants. Shown above are acceptable vs. non-acceptable burnishes. Use caution not to scrape away the bondable gold metal and never attempt this on a MMIC or IC pad.

Wire Looping Issues

All wires must have some loop for stress relief!



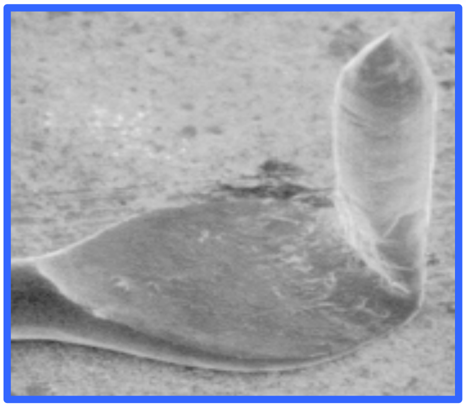


Verify there is sufficient clearance under the lid, the lid may oil can during pressurization cycles and/or there may be getters applied to the underside of the lid. Inspect to see wire does not contact the die edge. A straight line run on a wirebond is not permitted per TM 2017.

TM 2017 Para. 3.1.6.d

Ball Bonding (Tailing)

MARGINAL



Evidence of tailing which usually indicates the wire has gone soft. The subsequent ball is likely to be malformed. Potential exists for this wire to break loose in a hermetic cavity and cause a short, also inspect closely the next formed ball since it will probably be undersized. Ball bonds are not supposed to have a tail.

TM 2017 Para. 3.1.5.8.h

Course Notes

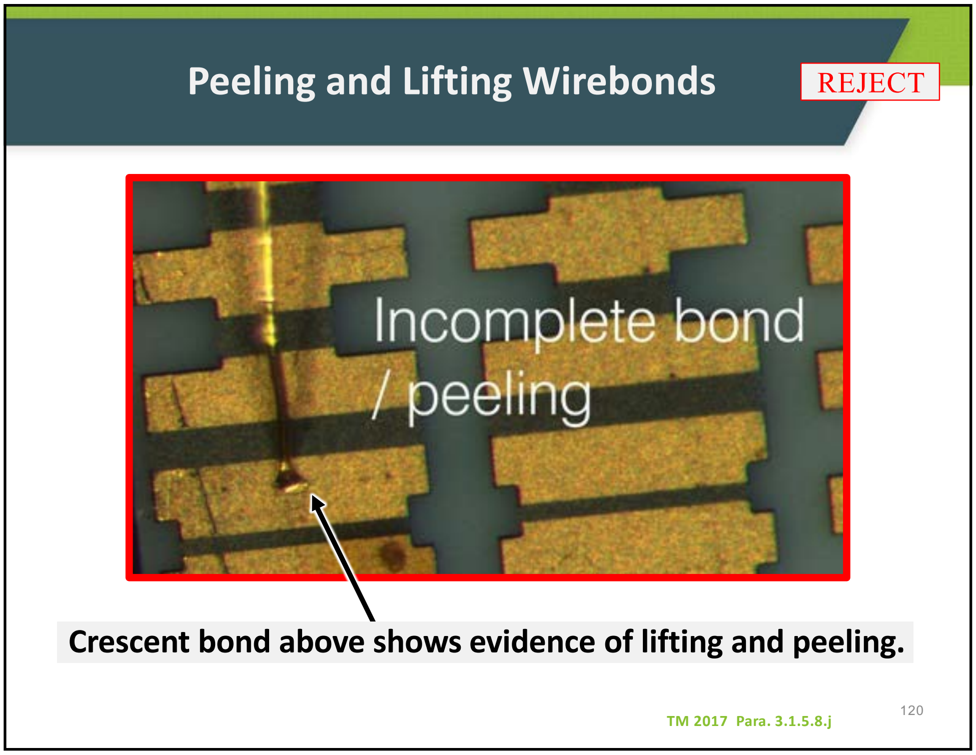
Wirebonds on Die Mounting Material

REJECT

Reject Bond on element attach adhesive

Bonds on element attach adhesive or on contaminated or foreign material is a REJECT.

TM 2017 Para. 3.1.5.8.i



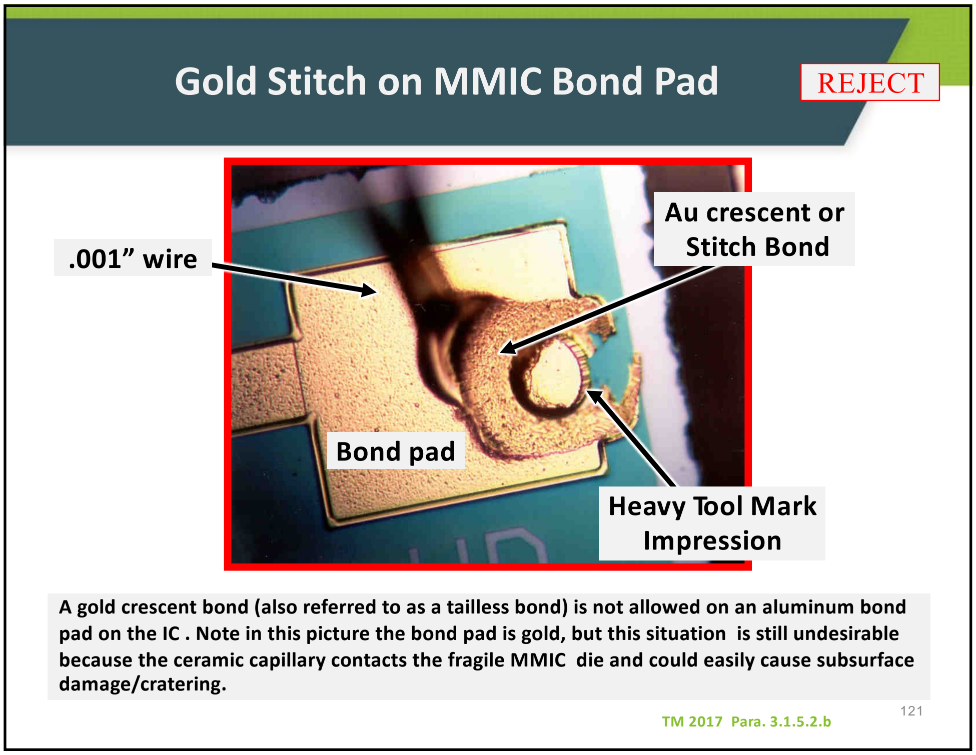
Peeling and Lifting Wirebonds

REJECT

Crescent bond above shows evidence of lifting and peeling.

TM 2017 Para. 3.1.5.8.j

Course Notes



Gold Stitch on MMIC Bond Pad

REJECT

.001” wire

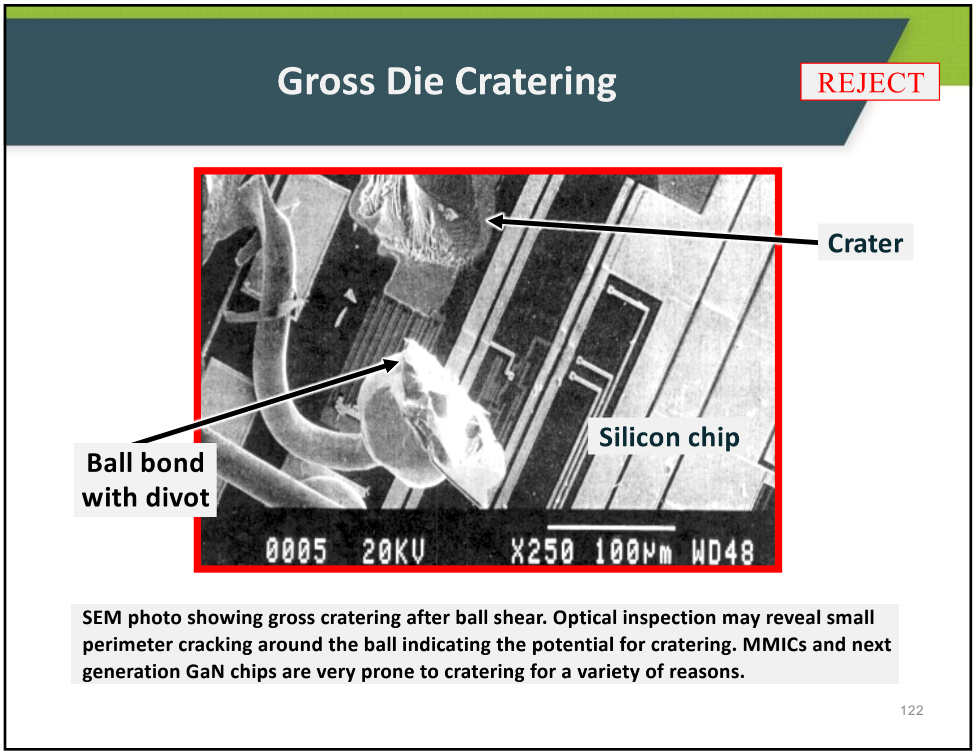
Au crescent or Stitch Bond

Bond pad

Heavy Tool Mark Impression

A gold crescent bond (also referred to as a tailless bond) is not allowed on an aluminum bond pad on the IC . Note in this picture the bond pad is gold, but this situation is still undesirable because the ceramic capillary contacts the fragile MMIC die and could easily cause subsurface damage/cratering.

TM 2017 Para. 3.1.5.2.b



Gross Die Cratering

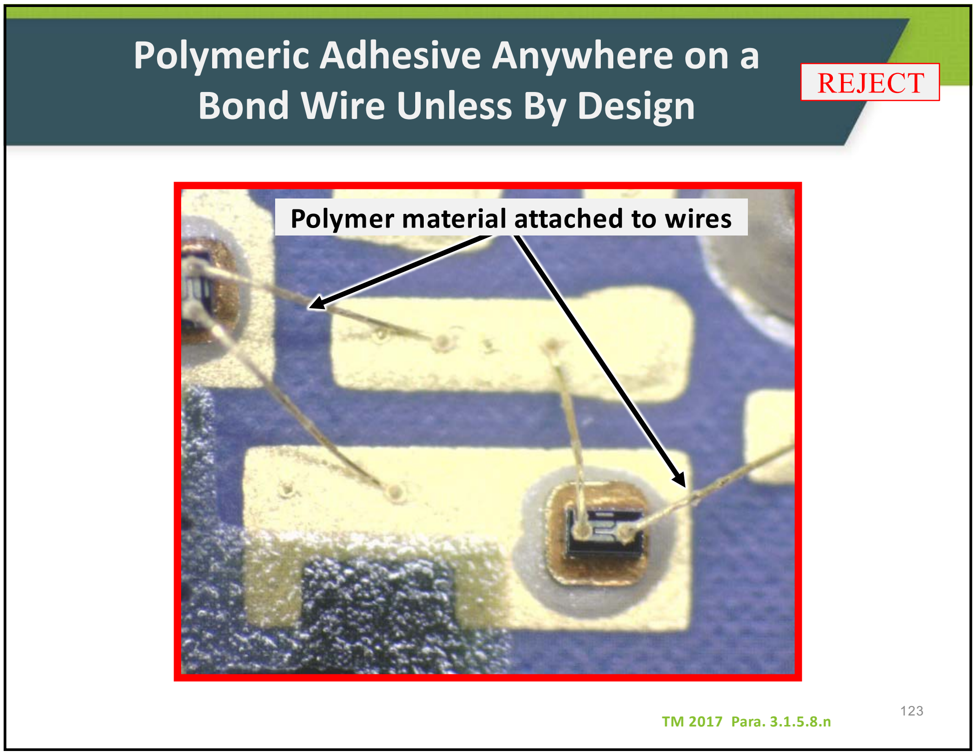
REJECT

Crater

Silicon chip

Ball bond with divot

SEM photo showing gross cratering after ball shear. Optical inspection may reveal small perimeter cracking around the ball indicating the potential for cratering. MMICs and next generation GaN chips are very prone to cratering for a variety of reasons.



Polymeric Adhesive Anywhere on a Bond Wire Unless By Design

REJECT

TM 2017 Para. 3.1.5.8.n

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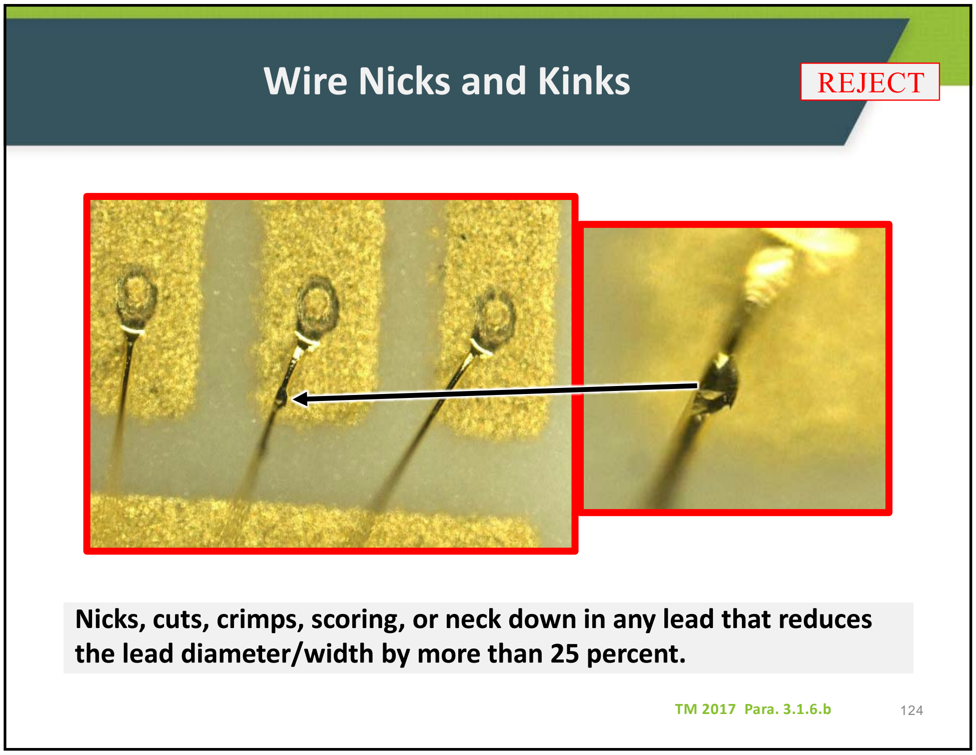

Wire Nicks and Kinks

REJECT

Nicks, cuts, crimps, scoring, or neck down in any lead that reduces the lead diameter/width by more than 25 percent.

TM 2017 Para. 3.1.6.b

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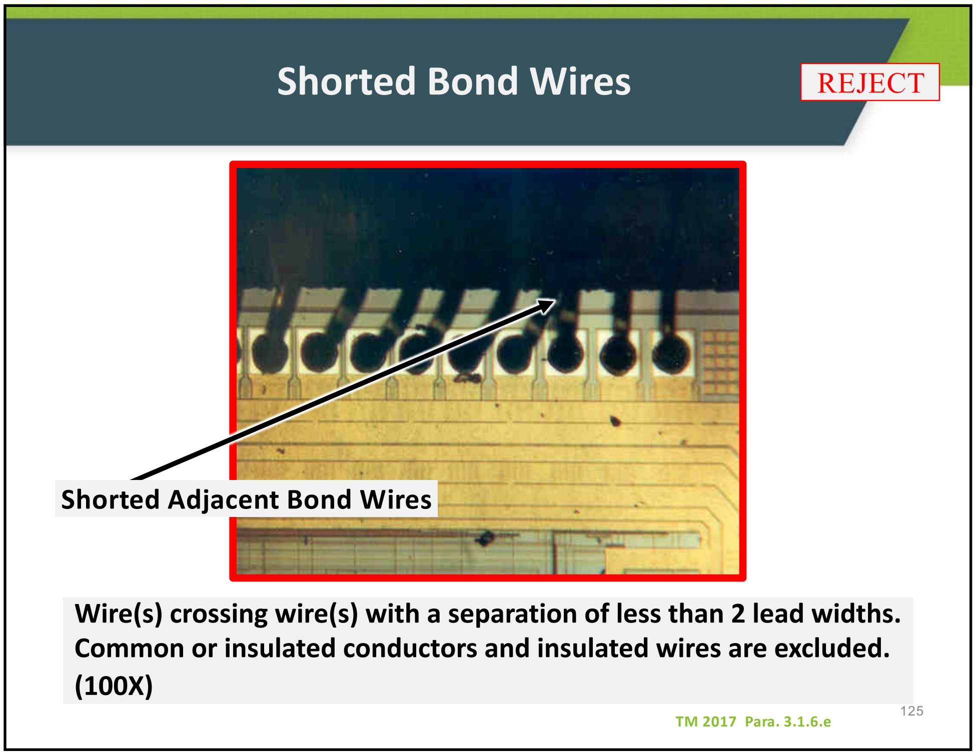
Course Notes



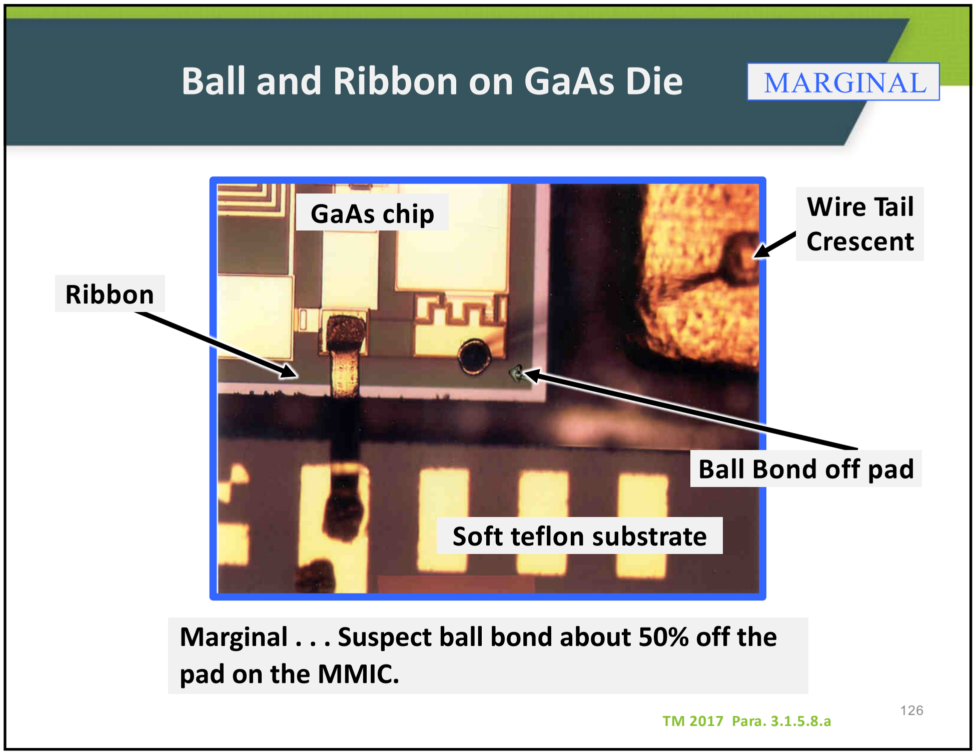
Shorted Bond Wires

REJECT

Shorted Adjacent Bond Wires

Wire(s) crossing wire(s) with a separation of less than 2 lead widths. Common or insulated conductors and insulated wires are excluded. (100X)

TM 2017 Para. 3.1.6.e



Ball and Ribbon on GaAs Die

MARGINAL

GaAs chip

Wire Tail Crescent

Ribbon

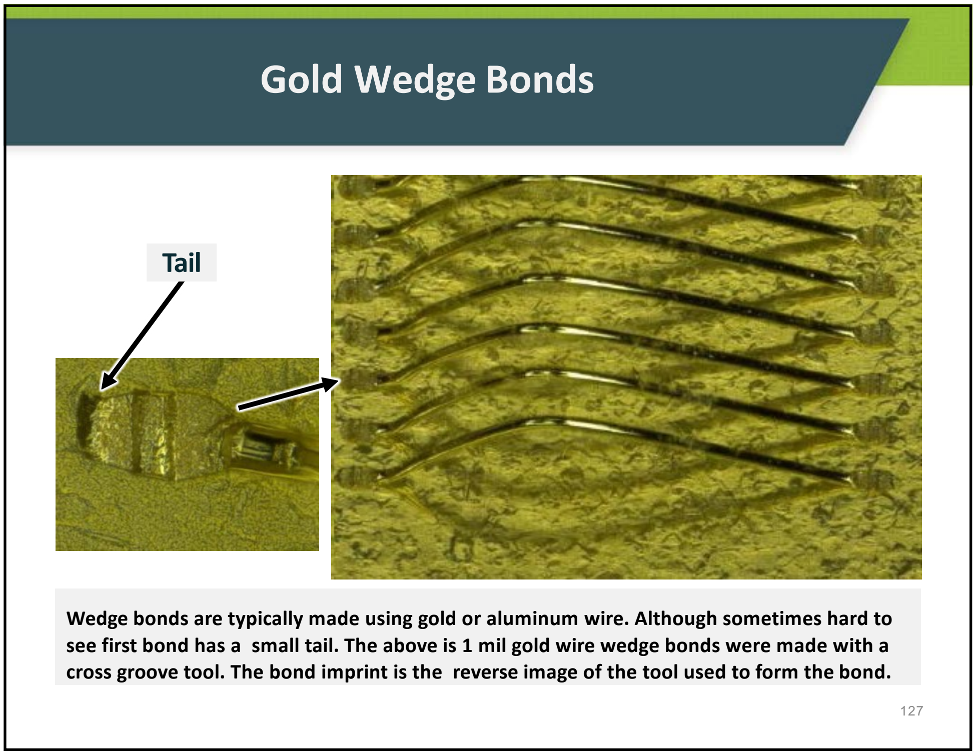
Ball Bond off pad

Soft teflon substrate

Marginal . . . Suspect ball bond about 50% off the pad on the MMIC.

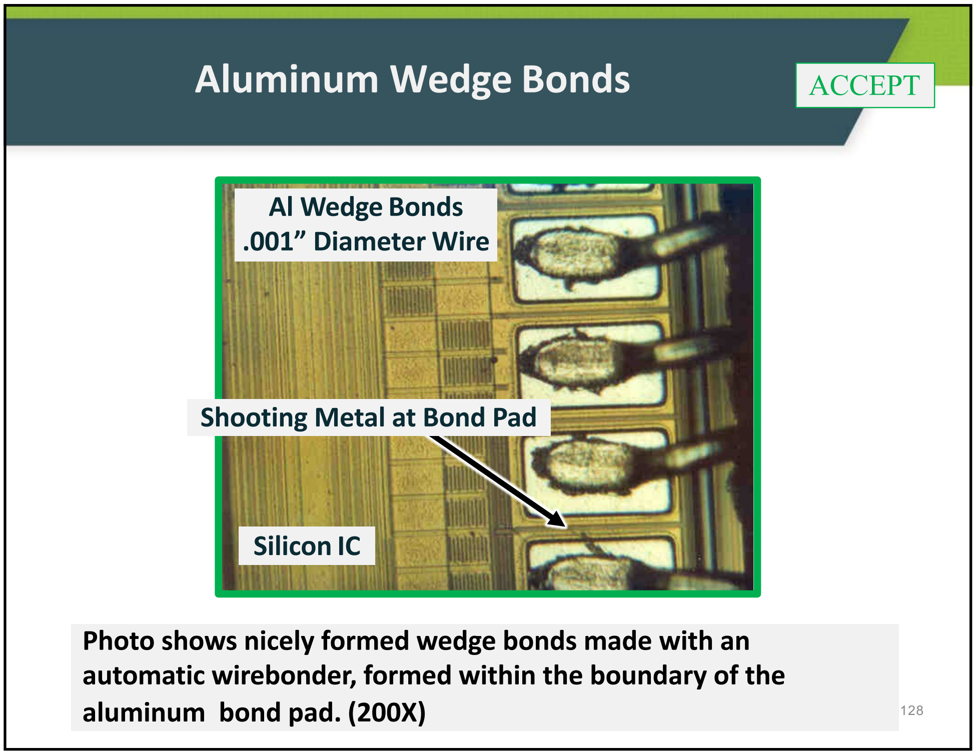
TM 2017 Para. 3.1.5.8.a

Course Notes



Gold Wedge Bonds

Wedge bonds are typically made using gold or aluminum wire. Although sometimes hard to see first bond has a small tail. The above is 1 mil gold wire wedge bonds were made with a cross groove tool. The bond imprint is the reverse image of the tool used to form the bond.

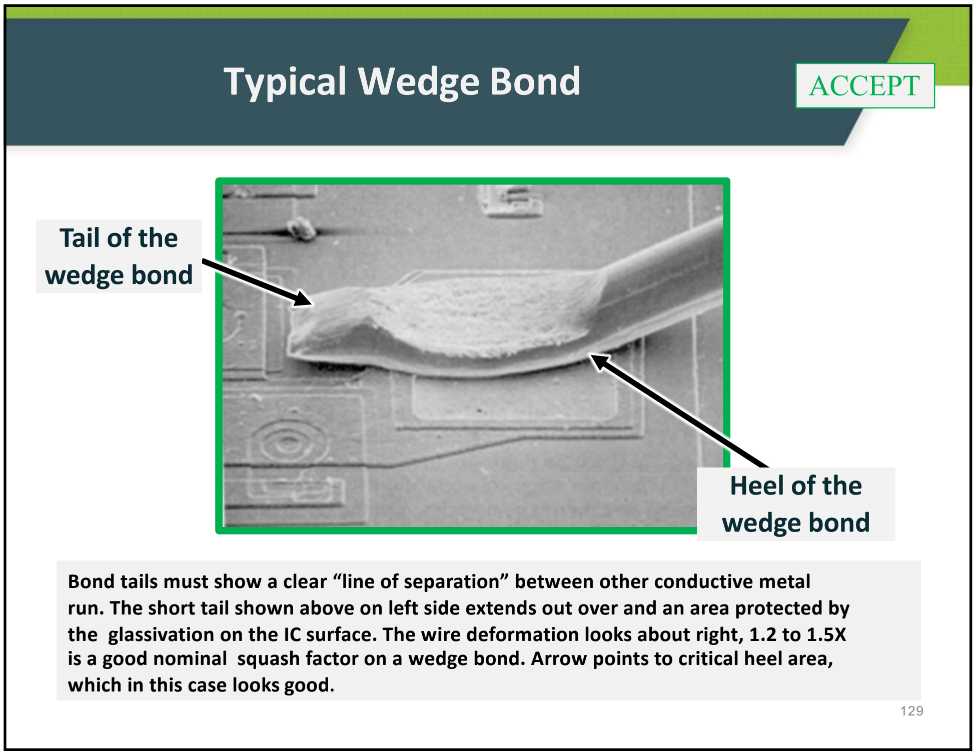


Aluminum Wedge Bonds

ACCEPT

Photo shows nicely formed wedge bonds made with an automatic wirebonder, formed within the boundary of the aluminum bond pad. (200X)

Course Notes



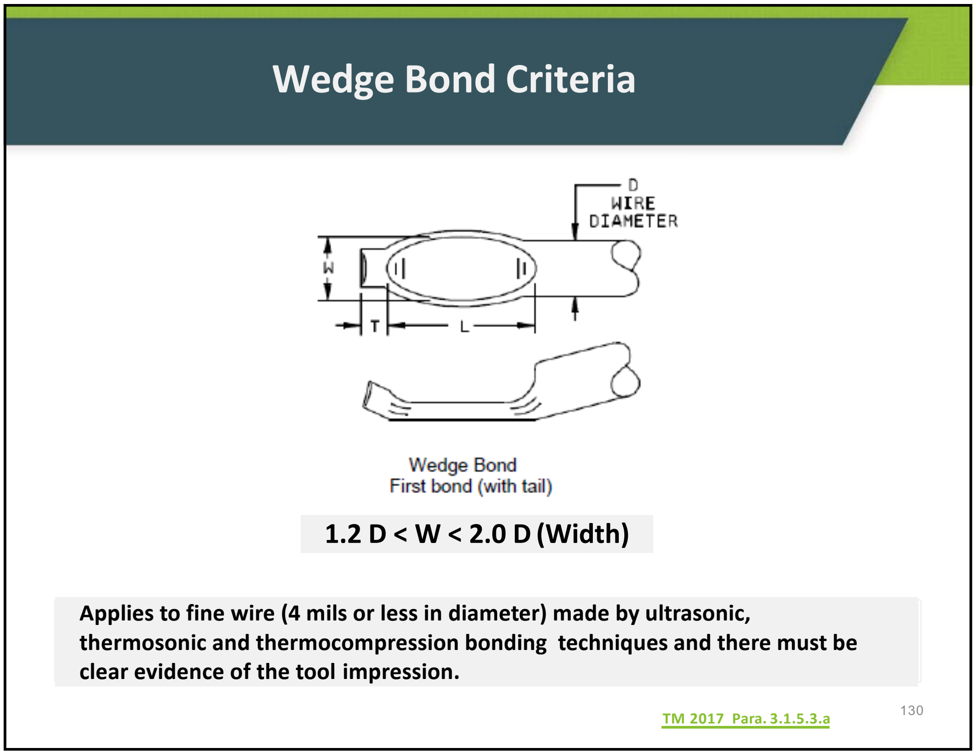
Typical Wedge Bond

ACCEPT

Tail of the wedge bond

Heel of the wedge bond

Bond tails must show a clear “line of separation” between other conductive metal run. The short tail shown above on left side extends out over and an area protected by the glassivation on the IC surface. The wire deformation looks about right, 1.2 to 1.5X is a good nominal squash factor on a wedge bond. Arrow points to critical heel area, which in this case looks good.



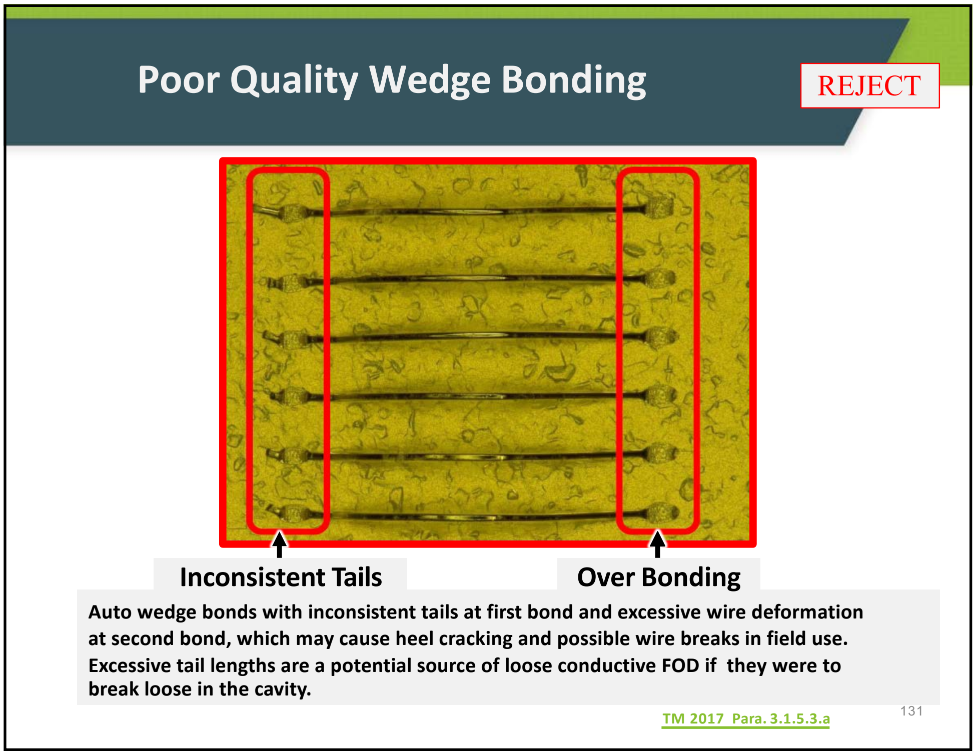
Wedge Bond Criteria

Wedge Bond
First bond (with tail)

1.2 D < W < 2.0 D (Width)

Applies to fine wire (4 mils or less in diameter) made by ultrasonic, thermosonic and thermocompression bonding techniques and there must be clear evidence of the tool impression.

TM 2017 Para. 3.1.5.3.a



Poor Quality Wedge Bonding

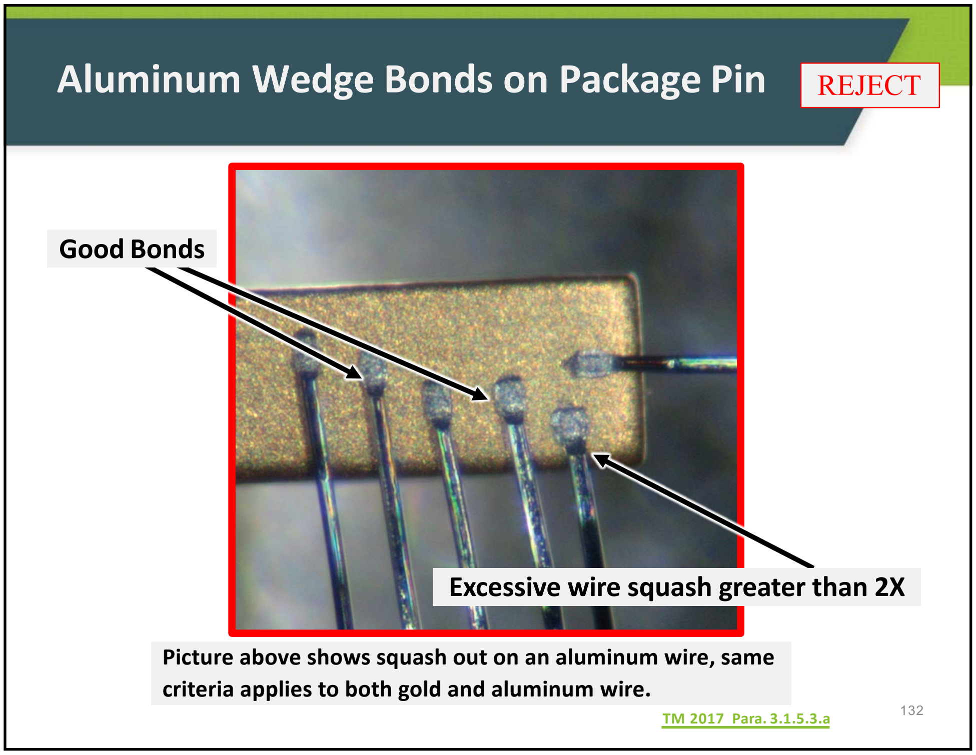
REJECT

Inconsistent Tails

Over Bonding

Auto wedge bonds with inconsistent tails at first bond and excessive wire deformation at second bond, which may cause heel cracking and possible wire breaks in field use. Excessive tail lengths are a potential source of loose conductive FOD if they were to break loose in the cavity.

TM 2017 Para. 3.1.5.3.a



Aluminum Wedge Bonds on Package Pin

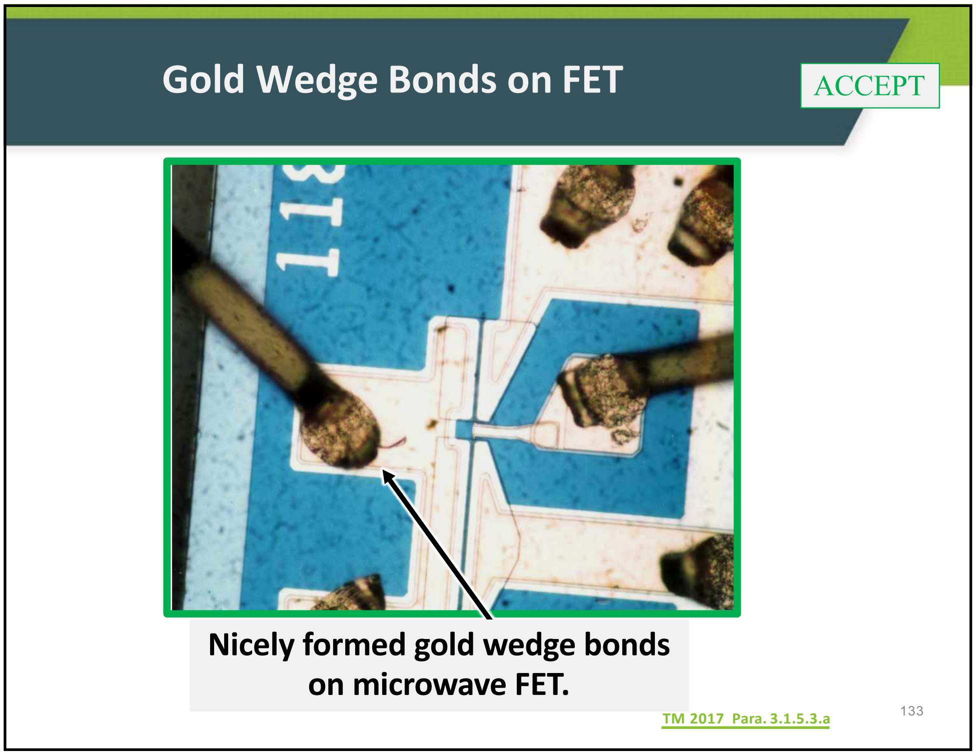
REJECT

Good Bonds

Excessive wire squash greater than 2X

Picture above shows squash out on an aluminum wire, same criteria applies to both gold and aluminum wire.

TM 2017 Para. 3.1.5.3.a

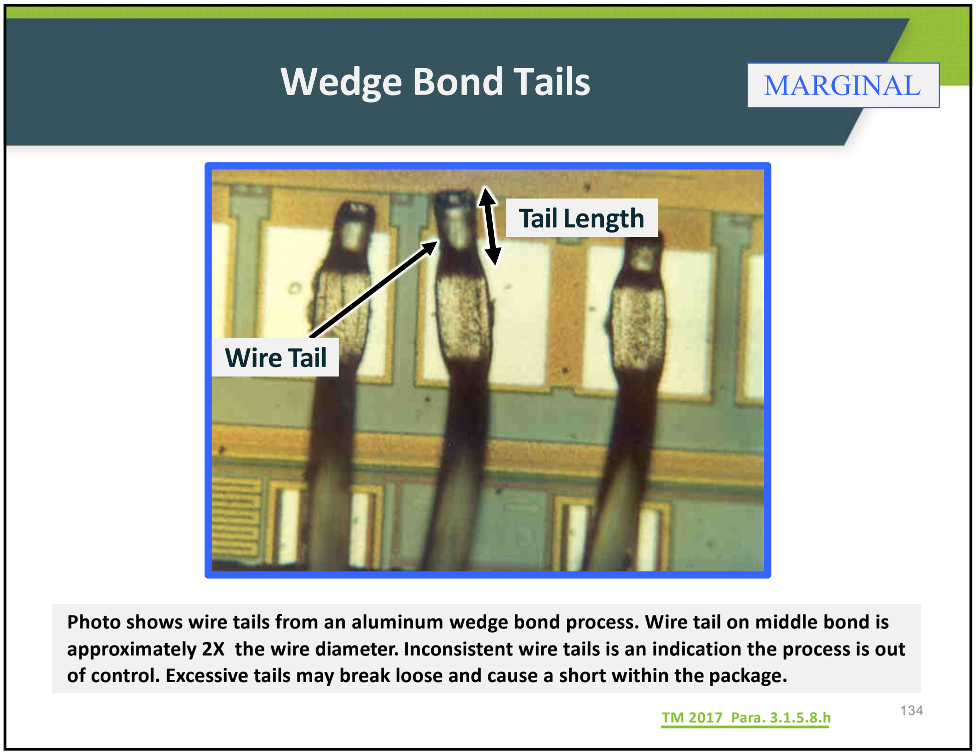


Gold Wedge Bonds on FET

ACCEPT

Nicely formed gold wedge bonds on microwave FET.

TM 2017 Para. 3.1.5.3.a



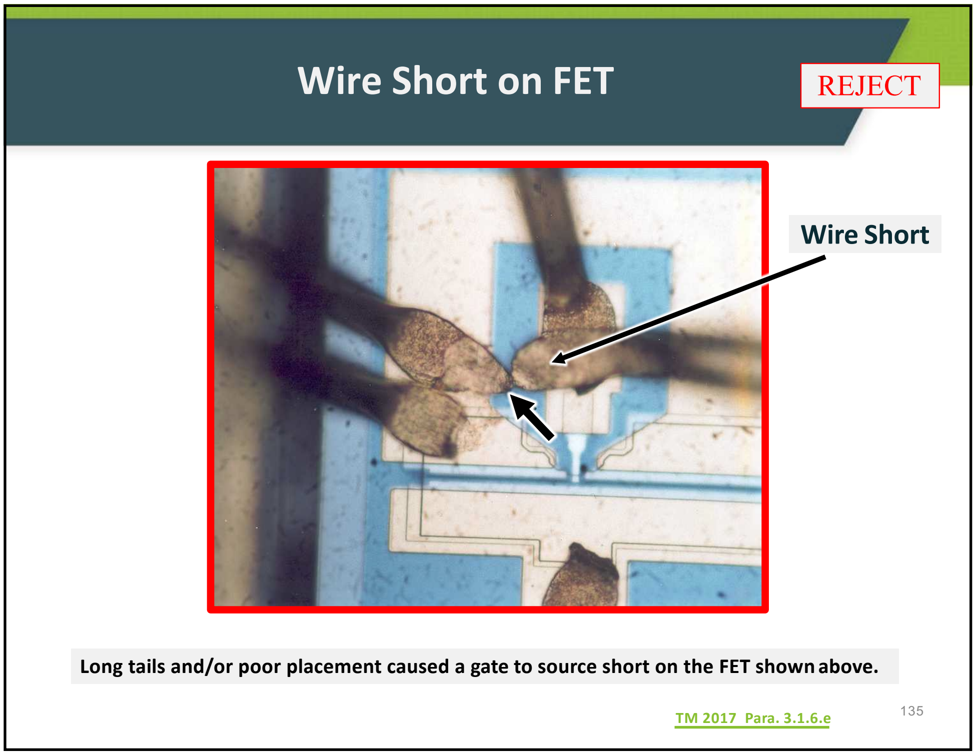
Wedge Bond Tails

MARGINAL

Photo shows wire tails from an aluminum wedge bond process. Wire tail on middle bond is approximately 2X the wire diameter. Inconsistent wire tails is an indication the process is out of control. Excessive tails may break loose and cause a short within the package.

TM 2017 Para. 3.1.5.8.h

Course Notes



Wire Short on FET

REJECT

Wire Short

Long tails and/or poor placement caused a gate to source short on the FET shown above.

TM 2017 Para. 3.1.6.e

Skidded Wire Footprint

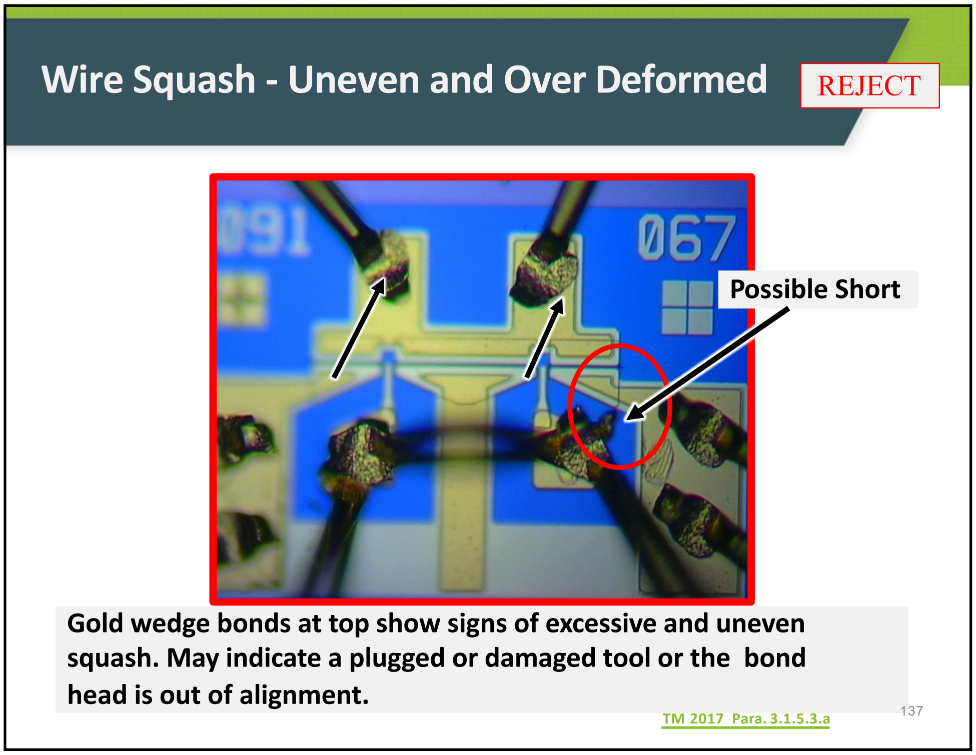
REJECT

Elongated Au wedge footprint

Deformed wedge bond footprint from automatic bonder, possibly due to a maladjusted clamp and/or wire slippage, stage movement or hand movement by operator during the bond cycle on a manual machine.

TM 2017 Para. 3.1.5.3.a

Course Notes



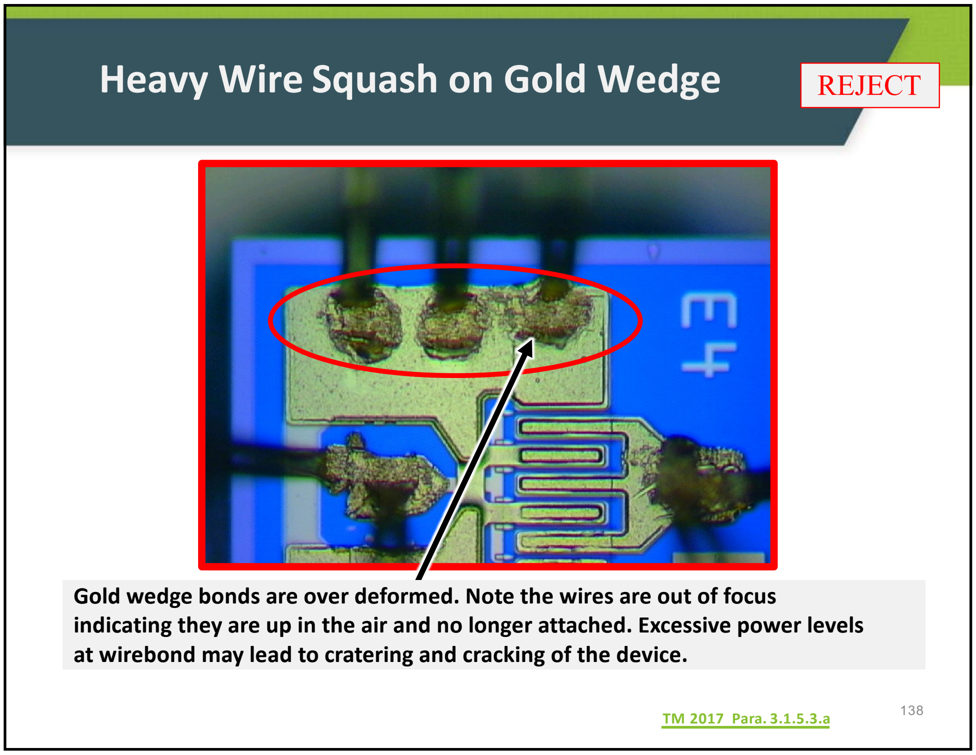
Wire Squash - Uneven and Over Deformed

REJECT

Possible Short

Gold wedge bonds at top show signs of excessive and uneven squash. May indicate a plugged or damaged tool or the bond head is out of alignment.

TM 2017 Para. 3.1.5.3.a

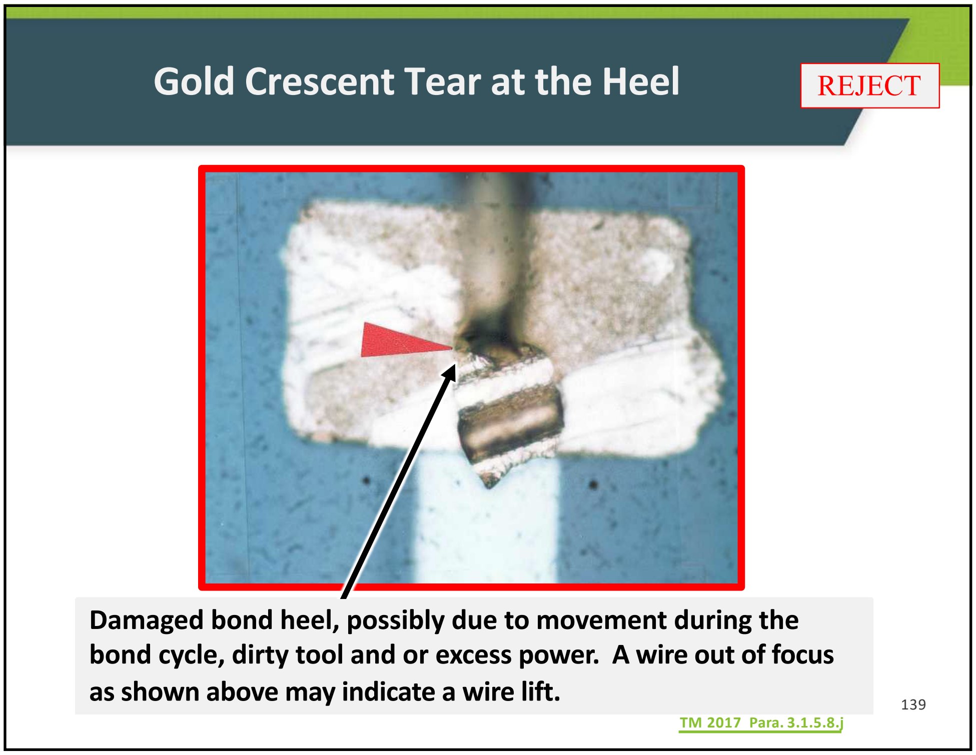


Heavy Wire Squash on Gold Wedge

REJECT

Gold wedge bonds are over deformed. Note the wires are out of focus indicating they are up in the air and no longer attached. Excessive power levels at wirebond may lead to cratering and cracking of the device.

TM 2017 Para. 3.1.5.3.a

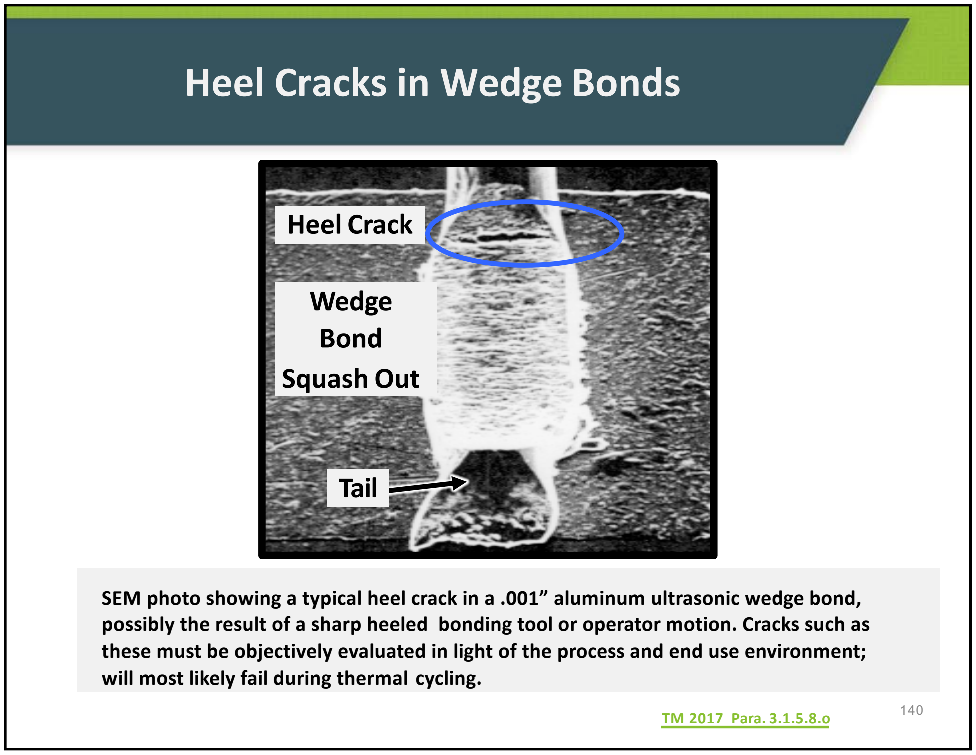


Gold Crescent Tear at the Heel

REJECT

Damaged bond heel, possibly due to movement during the bond cycle, dirty tool and or excess power. A wire out of focus as shown above may indicate a wire lift.

TM 2017 Para. 3.1.5.8.j



Heel Cracks in Wedge Bonds

Heel Crack

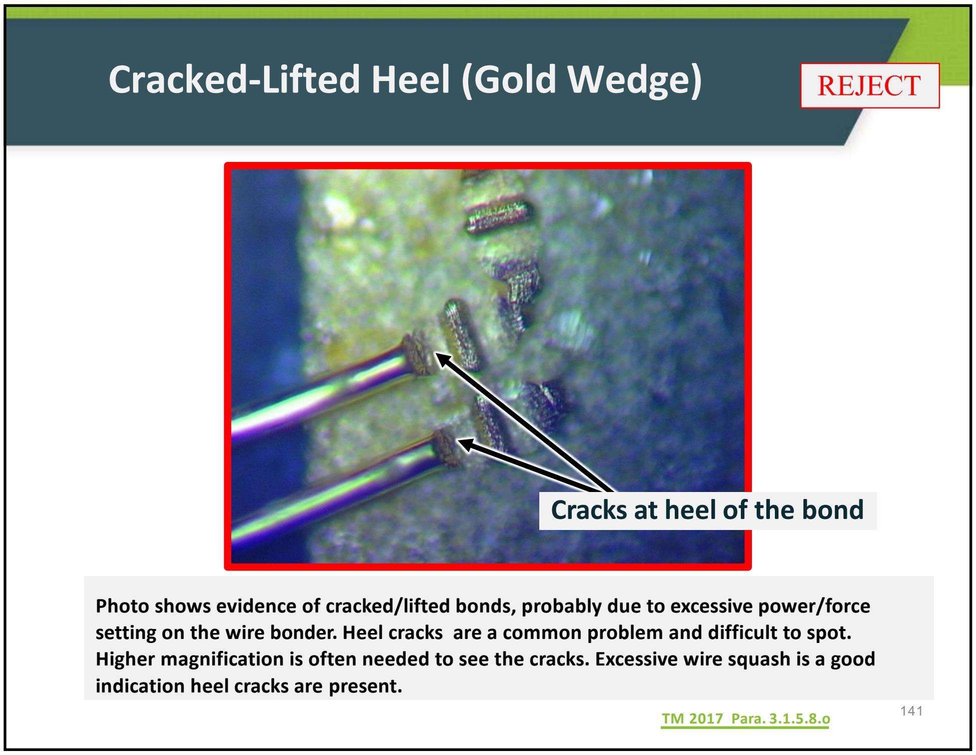
Wedge Bond Squash Out

Tail

SEM photo showing a typical heel crack in a .001” aluminum ultrasonic wedge bond, possibly the result of a sharp heeled bonding tool or operator motion. Cracks such as these must be objectively evaluated in light of the process and end use environment; will most likely fail during thermal cycling.

TM 2017 Para. 3.1.5.8.o

Course Notes



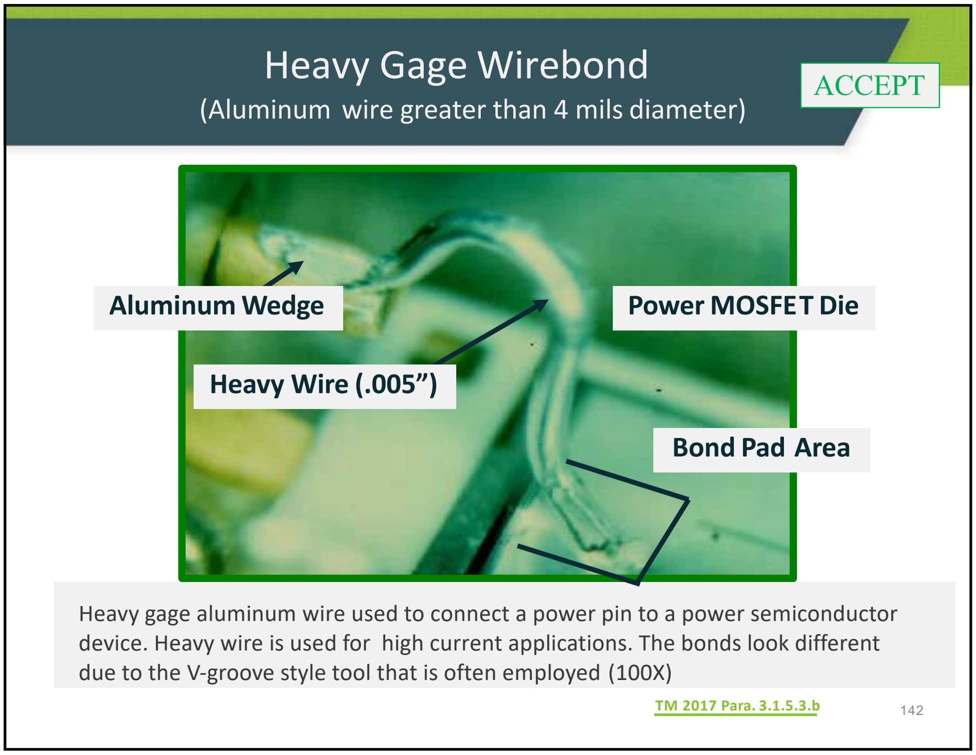
Cracked-Lifted Heel (Gold Wedge)

REJECT

Cracks at heel of the bond

Photo shows evidence of cracked/lifted bonds, probably due to excessive power/force setting on the wire bonder. Heel cracks are a common problem and difficult to spot. Higher magnification is often needed to see the cracks. Excessive wire squash is a good indication heel cracks are present.

TM 2017 Para. 3.1.5.8.o



Heavy Gage Wirebond

(Aluminum wire greater than 4 mils diameter)

ACCEPT

Aluminum Wedge

Power MOSFET Die

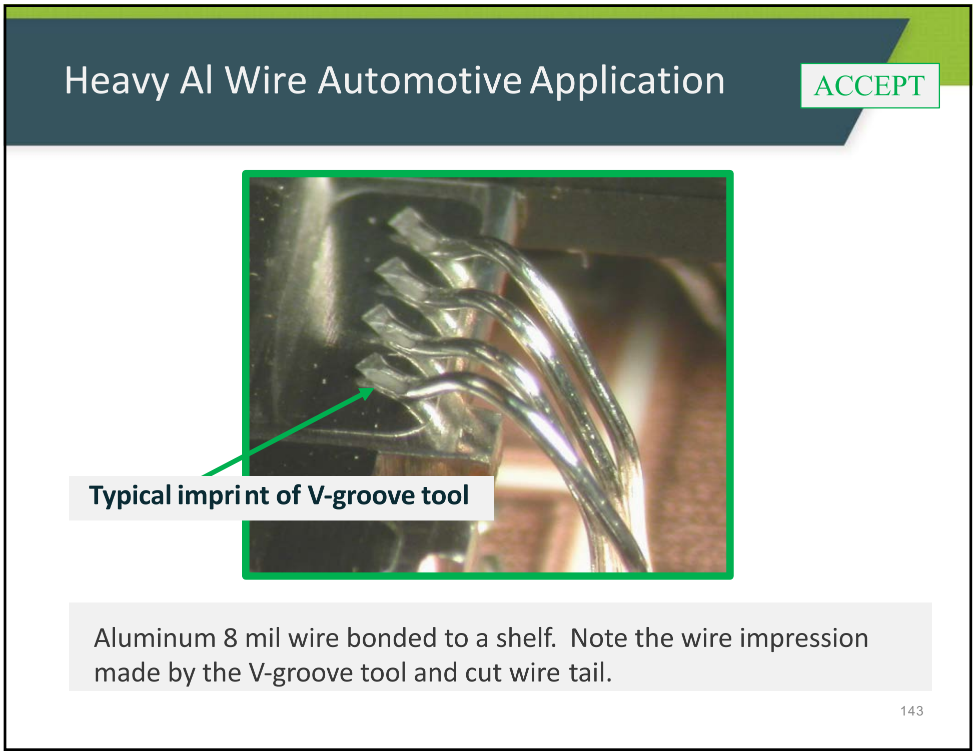
Heavy Wire (.005”)

Bond Pad Area

Heavy gage aluminum wire used to connect a power pin to a power semiconductor device. Heavy wire is used for high current applications. The bonds look different due to the V-groove style tool that is often employed (100X)

TM 2017 Para. 3.1.5.3.b

Course Notes

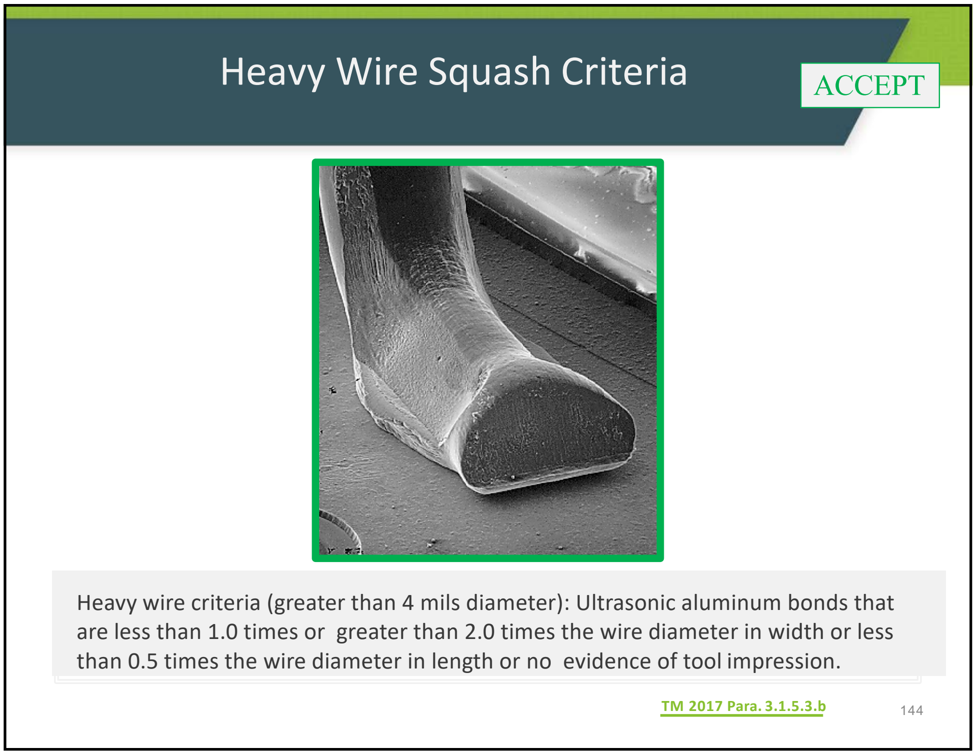


Heavy Al Wire Automotive Application

ACCEPT

Typical imprint of V-groove tool

Aluminum 8 mil wire bonded to a shelf. Note the wire impression made by the V-groove tool and cut wire tail.



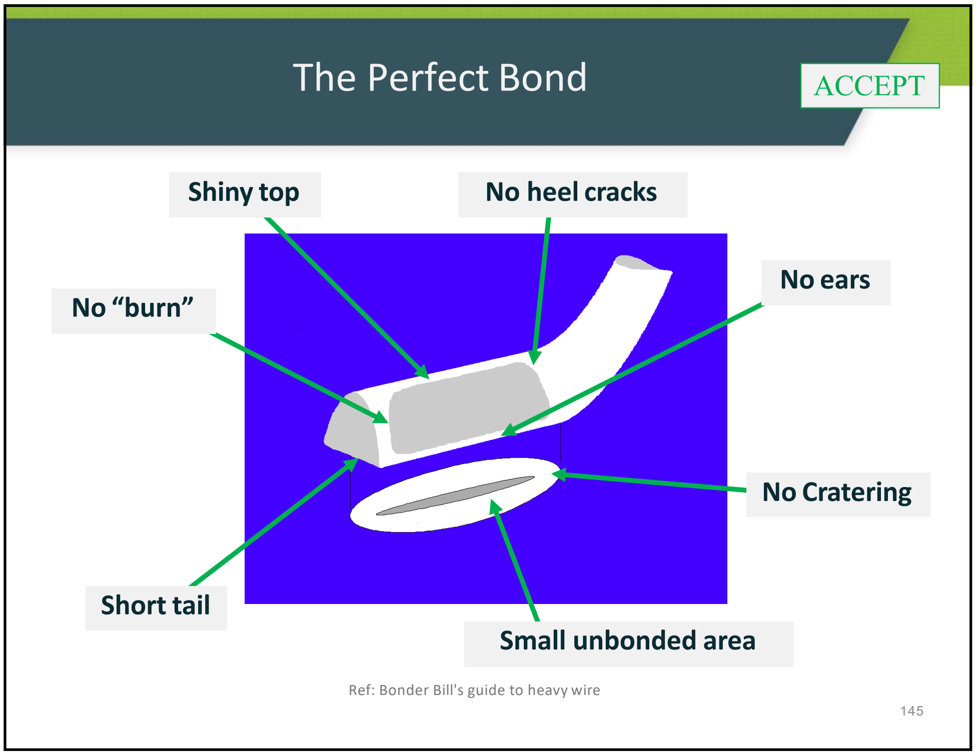
Heavy Wire Squash Criteria

ACCEPT

Heavy wire criteria (greater than 4 mils diameter): Ultrasonic aluminum bonds that are less than 1.0 times or greater than 2.0 times the wire diameter in width or less than 0.5 times the wire diameter in length or no evidence of tool impression.

TM 2017 Para. 3.1.5.3.b

Course Notes



The Perfect Bond

ACCEPT

Shiny top

No heel cracks

No "burn"

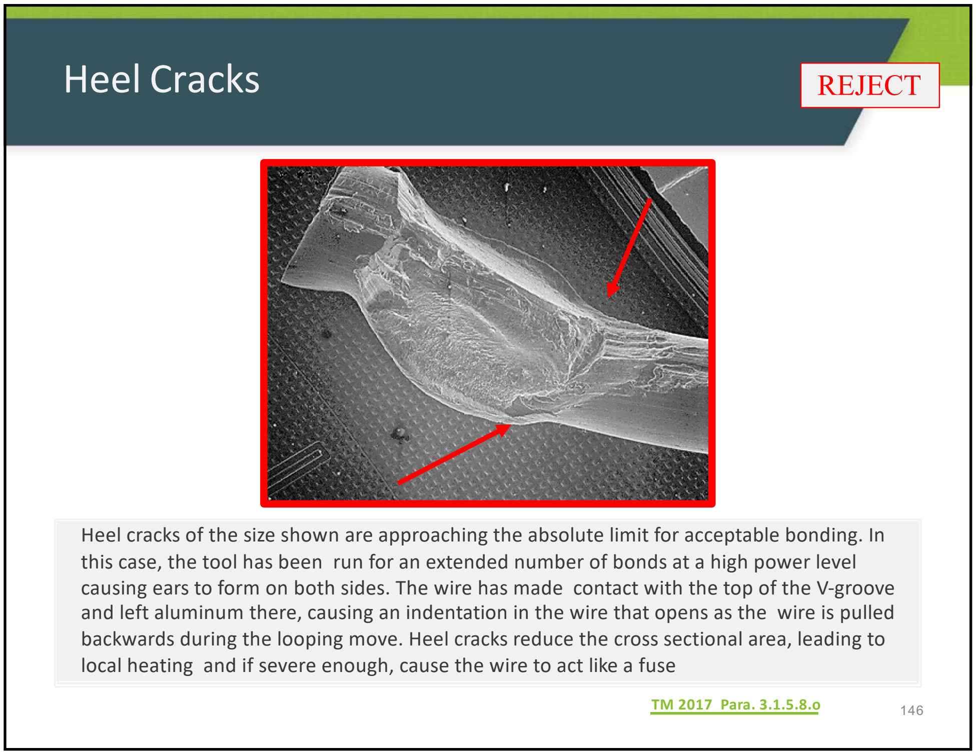
No ears

No Cratering

Short tail

Small unbonded area

Ref: Bonder Bill's guide to heavy wire



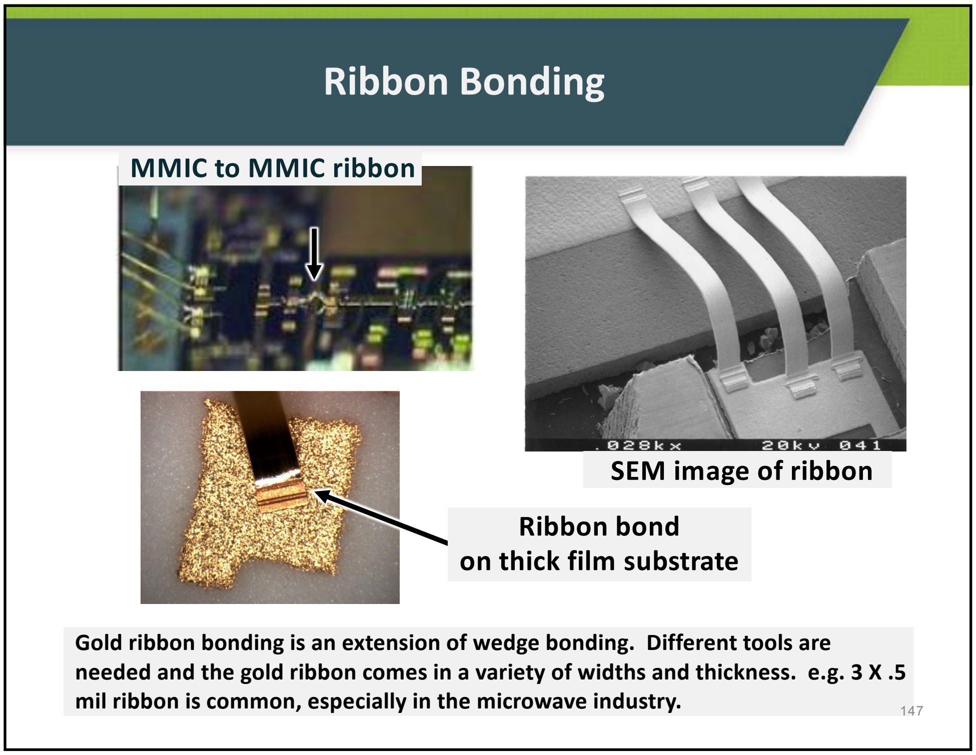
Heel Cracks

REJECT

Heel cracks of the size shown are approaching the absolute limit for acceptable bonding. In this case, the tool has been run for an extended number of bonds at a high power level causing ears to form on both sides. The wire has made contact with the top of the V-groove and left aluminum there, causing an indentation in the wire that opens as the wire is pulled backwards during the looping move. Heel cracks reduce the cross sectional area, leading to local heating and if severe enough, cause the wire to act like a fuse

TM 2017 Para. 3.1.5.8.o

Course Notes



Ribbon Bonding

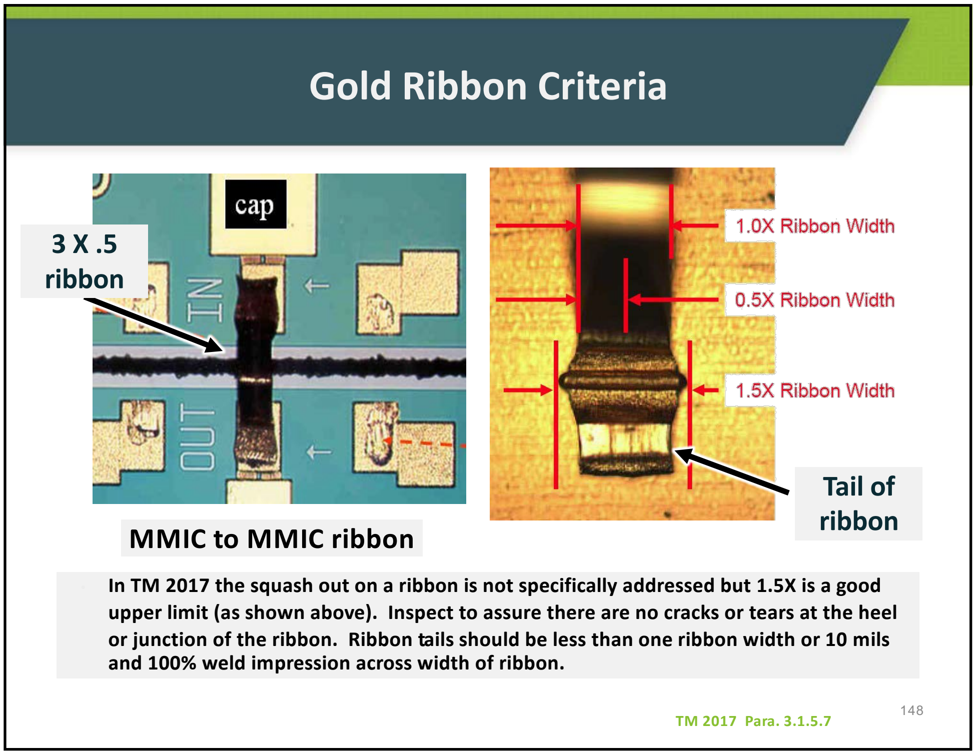
MMIC to MMIC ribbon

SEM image of ribbon

Ribbon bond
on thick film substrate

Gold ribbon bonding is an extension of wedge bonding. Different tools are needed and the gold ribbon comes in a variety of widths and thickness. e.g. 3 X .5 mil ribbon is common, especially in the microwave industry.

147



Gold Ribbon Criteria

3 X .5
ribbon

MMIC to MMIC ribbon

1.0X Ribbon Width

0.5X Ribbon Width

1.5X Ribbon Width

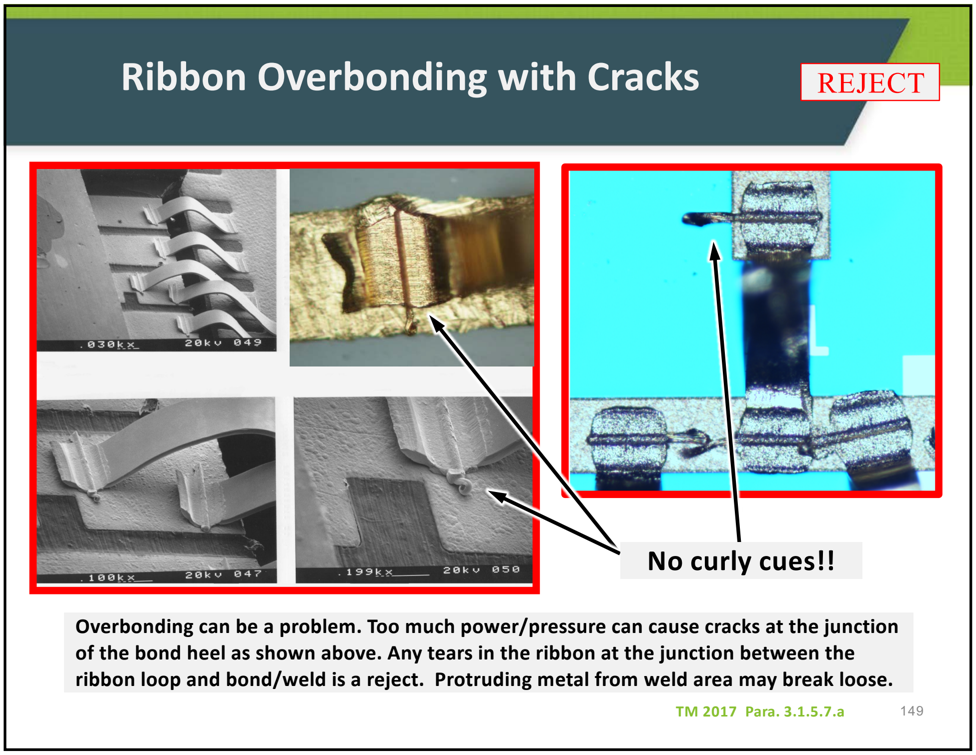
Tail of
ribbon

In TM 2017 the squash out on a ribbon is not specifically addressed but 1.5X is a good upper limit (as shown above). Inspect to assure there are no cracks or tears at the heel or junction of the ribbon. Ribbon tails should be less than one ribbon width or 10 mils and 100% weld impression across width of ribbon.

TM 2017 Para. 3.1.5.7

148

Course Notes



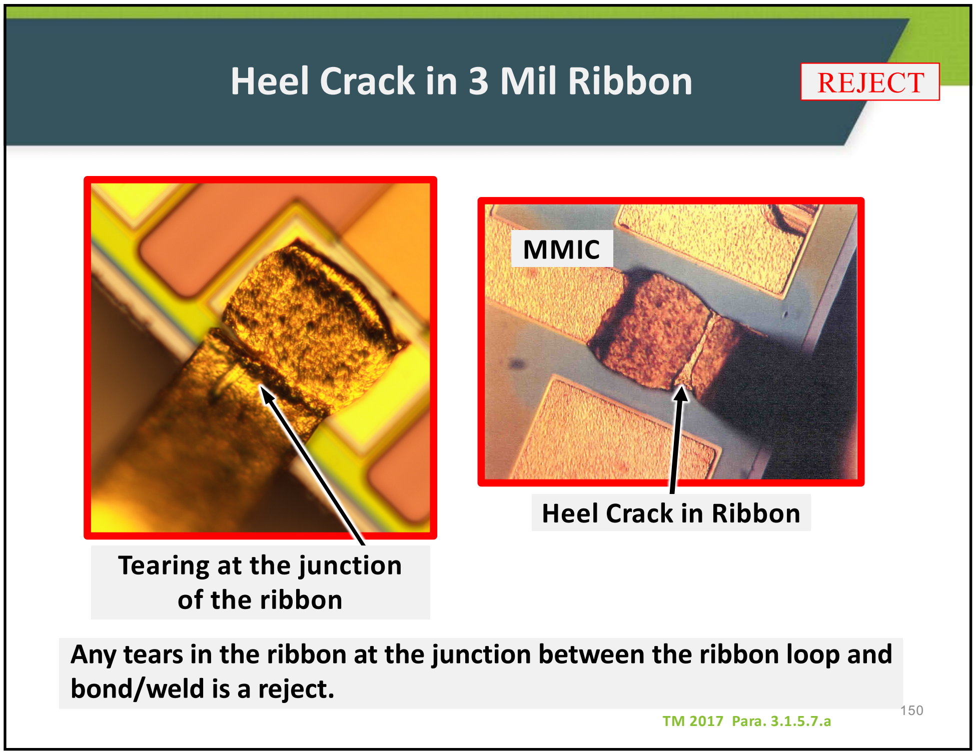
Ribbon Overbonding with Cracks

REJECT

No curly cues!!

Overbonding can be a problem. Too much power/pressure can cause cracks at the junction of the bond heel as shown above. Any tears in the ribbon at the junction between the ribbon loop and bond/weld is a reject. Protruding metal from weld area may break loose.

TM 2017 Para. 3.1.5.7.a



Heel Crack in 3 Mil Ribbon

REJECT

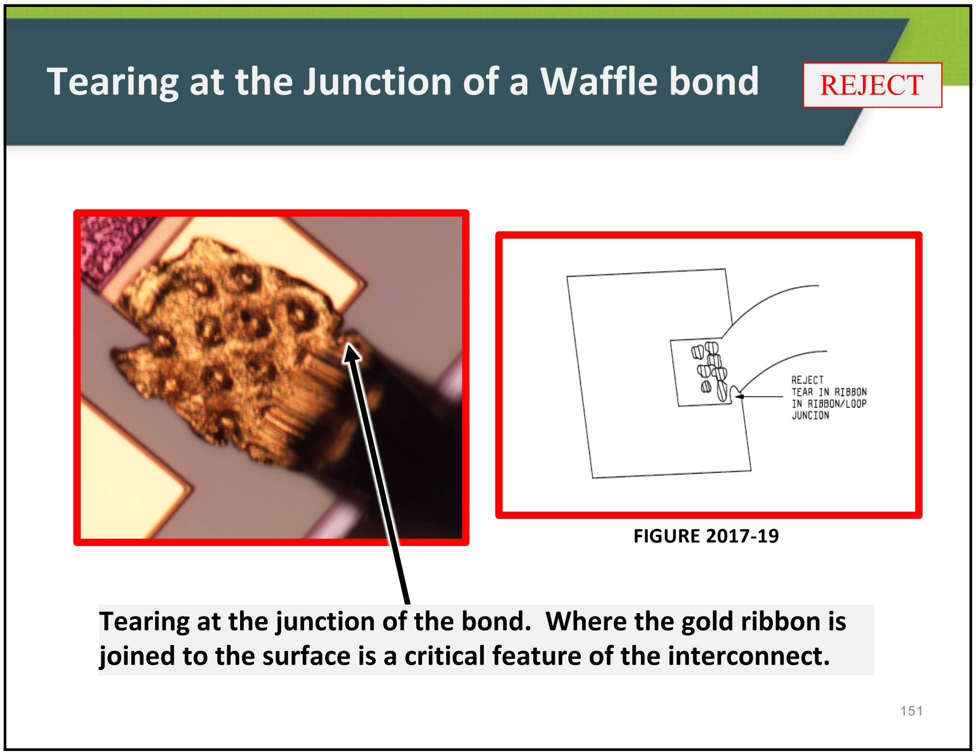
Tearing at the junction of the ribbon

Heel Crack in Ribbon

Any tears in the ribbon at the junction between the ribbon loop and bond/weld is a reject.

TM 2017 Para. 3.1.5.7.a

Course Notes

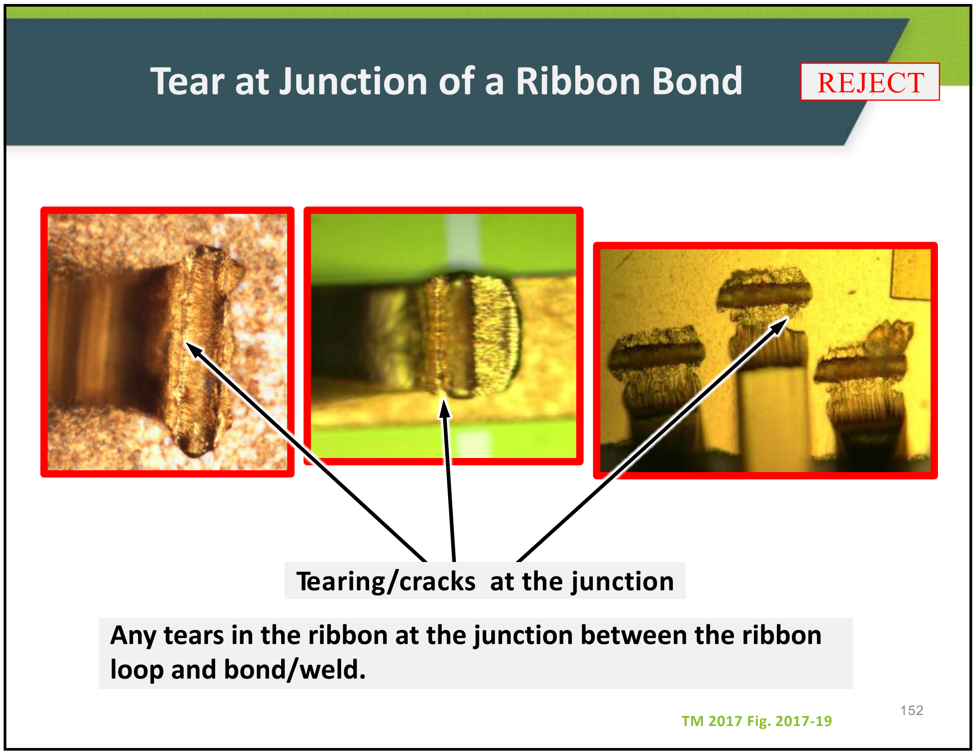


Tearing at the Junction of a Waffle bond

REJECT

FIGURE 2017-19

Tearing at the junction of the bond. Where the gold ribbon is joined to the surface is a critical feature of the interconnect.



Tear at Junction of a Ribbon Bond

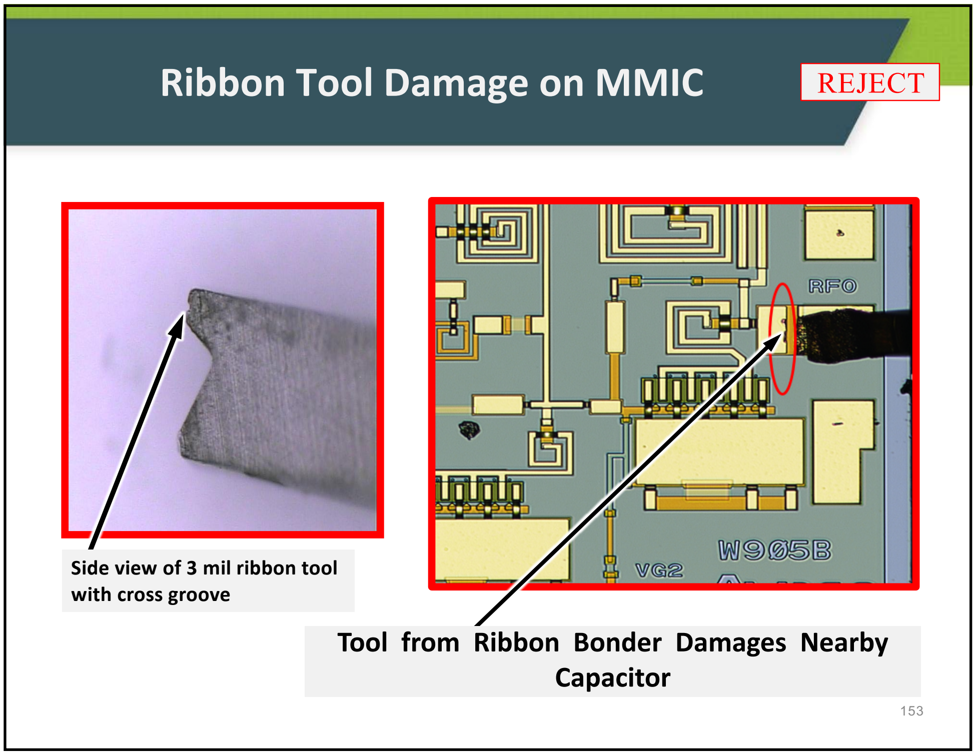
REJECT

Tearing/cracks at the junction

Any tears in the ribbon at the junction between the ribbon loop and bond/weld.

TM 2017 Fig. 2017-19

Course Notes

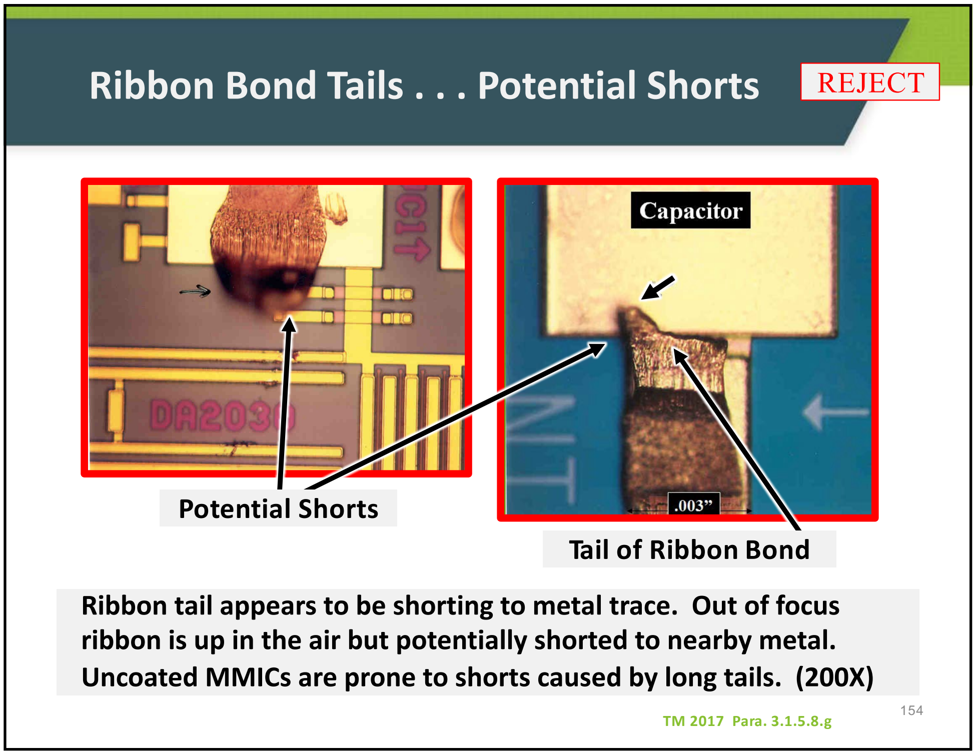


Ribbon Tool Damage on MMIC

REJECT

Side view of 3 mil ribbon tool with cross groove

Tool from Ribbon Bonder Damages Nearby Capacitor



Ribbon Bond Tails . . . Potential Shorts

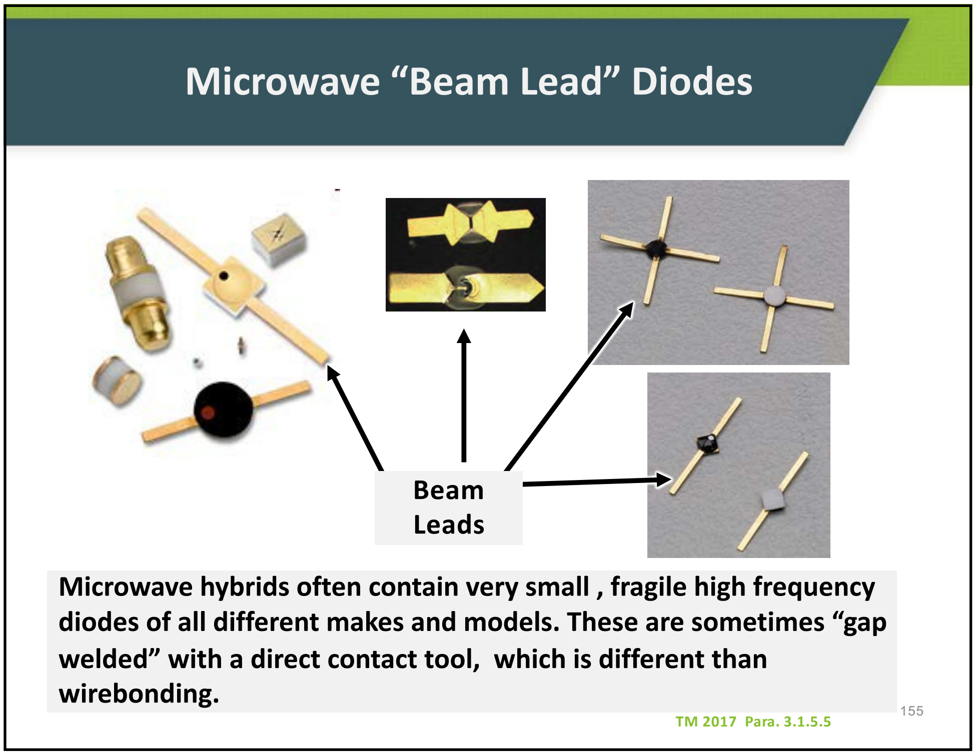
REJECT

Potential Shorts

Tail of Ribbon Bond

Ribbon tail appears to be shorting to metal trace. Out of focus ribbon is up in the air but potentially shorted to nearby metal. Uncoated MMICs are prone to shorts caused by long tails. (200X)

TM 2017 Para. 3.1.5.8.g

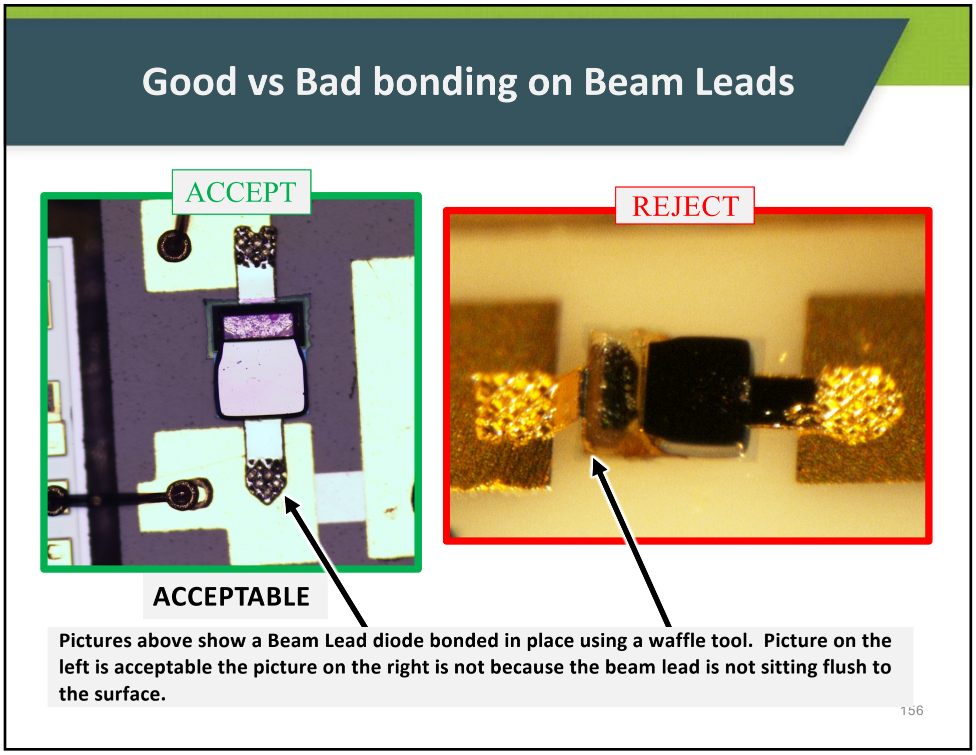


Microwave "Beam Lead" Diodes

Beam Leads

Microwave hybrids often contain very small , fragile high frequency diodes of all different makes and models. These are sometimes "gap welded" with a direct contact tool, which is different than wirebonding.

TM 2017 Para. 3.1.5.5



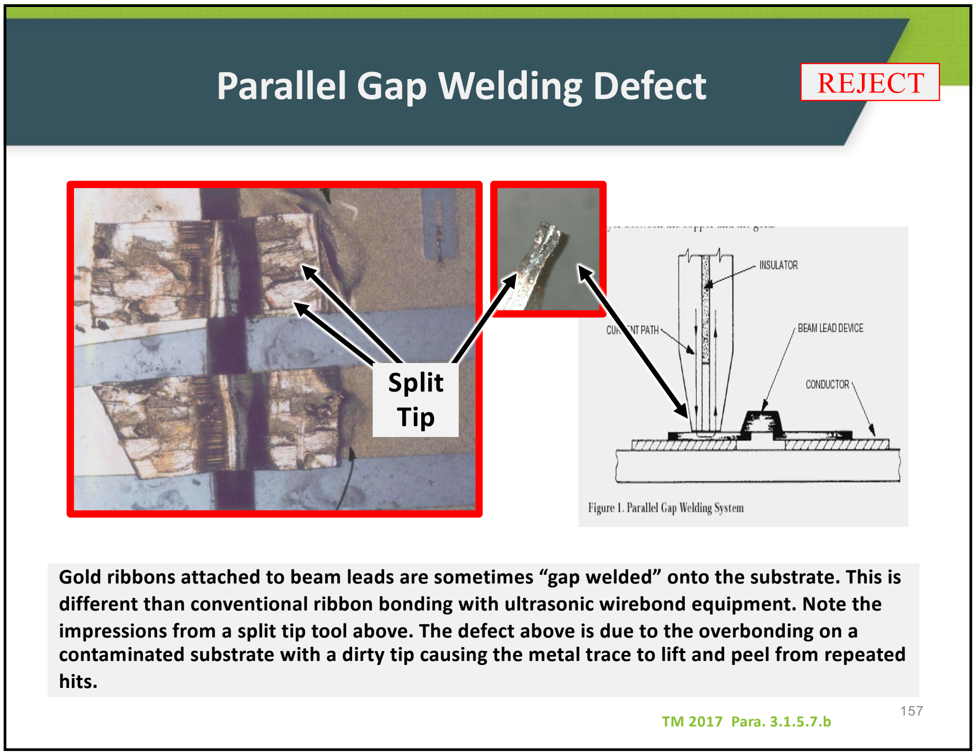
Good vs Bad bonding on Beam Leads

ACCEPT

REJECT

ACCEPTABLE

Pictures above show a Beam Lead diode bonded in place using a waffle tool. Picture on the left is acceptable the picture on the right is not because the beam lead is not sitting flush to the surface.



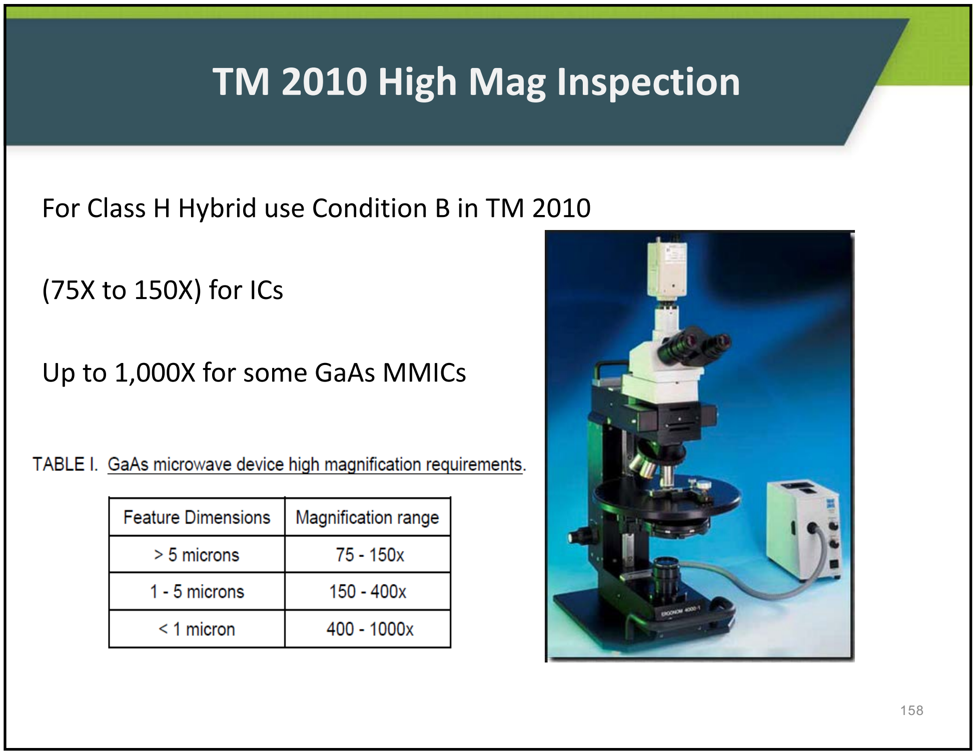
Parallel Gap Welding Defect

REJECT

Figure 1. Parallel Gap Welding System

Gold ribbons attached to beam leads are sometimes "gap welded" onto the substrate. This is different than conventional ribbon bonding with ultrasonic wirebond equipment. Note the impressions from a split tip tool above. The defect above is due to the overbonding on a contaminated substrate with a dirty tip causing the metal trace to lift and peel from repeated hits.

TM 2017 Para. 3.1.5.7.b



TM 2010 High Mag Inspection

For Class H Hybrid use Condition B in TM 2010

(75X to 150X) for ICs

Up to 1,000X for some GaAs MMICs

TABLE I. GaAs microwave device high magnification requirements.

Feature Dimensions	Magnification range
> 5 microns	75 - 150x
1 - 5 microns	150 - 400x
< 1 micron	400 - 1000x

Dimensions and Measurements

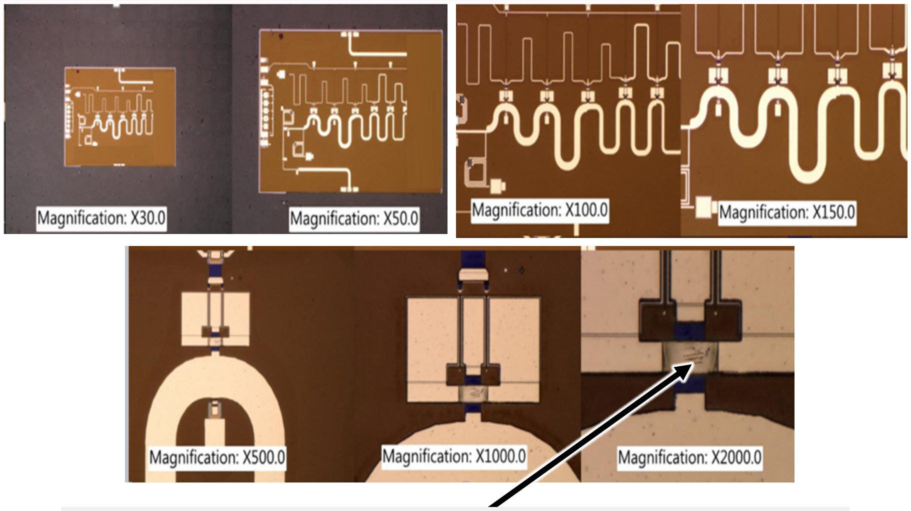
A word about length: The term mil and micron are commonly used. Both refer to a unit of length.

A mil is one thousandth of an inch.
1 mil = 0.001 inch = 25.4 microns
A micron (µm) is one millionth of a meter.
1 micron (1 µm) = 1/1,000,000 meter = 10,000 Å = 0.04 mils

Typical dimensions of components found within a Hybrid circuit:

Minimum dist from top of package to pin	40 mils
Thickness of a ceramic substrate	25 mils
Width of a Thick Film Conductor	10 mils
Gold Wire diameter	1 mil
Thickness of to Au Plating	50 microinches
Transistor gate length on IC	.22 microns

MMIC Die Inspect Low to High Mag Pics



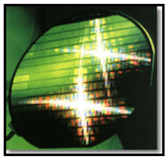
High mag is often needed to identify tiny features on MMIC die surface. In this case the small blemish on top of the air bridge is OK …its an artifact of the plating process.

Optical Microscopes

- Bright Field
  - Light goes directly through the objective lens and reflects from the sample’s surface. Bright view is used to view an object’s surface.
- Dark Field
  - Light is directed to the sample at a low angle. By adjusting the focus, an observer sees reflections from the surface and objects below the surface if the sample’s matrix is transparent. Dark filed can be used to determine if a particle is embedded.
- Polarized Light
  - Polarized light is directed to the sample. Interference contrast is used to find objects.

Silicon IC Wafer Terminology

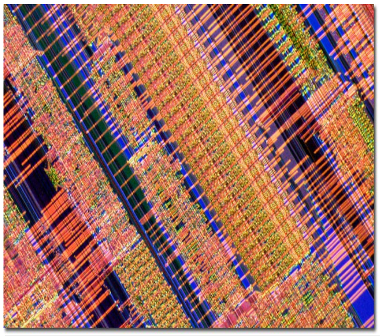
- SEMICONDUCTOR - A solid material with resistivity midway between that of a conductor and an insulator. Silicon, which comes from sand, is the most commonly used semiconductor.



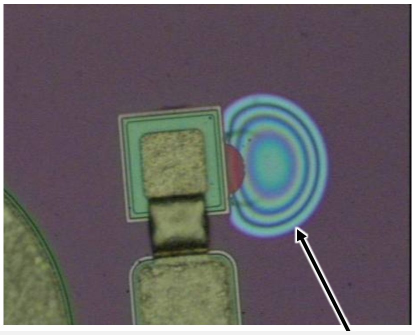
- SILICON WAFER - A thin disk of silicon, up to 18 inches in diameter. Integrated circuits (ICs) are created on its mirror-shiny surface, then cut with diamond saws into individual chips.
- CHIP - A small piece of semiconducting material (usually silicon) on which an integrated circuit is embedded. A typical chip is less than 1 square inch and can contain millions of electronic components. Its purpose is to electronically process, store and move information.
- INTEGRATED CIRCUIT (IC) - Large numbers of integrated transistors and other circuit elements, which are built onto an individual chip to perform a particular function or task. i.e. memory chips, microprocessors etc.

Course Notes

Color Fringing and High Mag Die Inspect



Modern day IC as seen through a high powered microscope

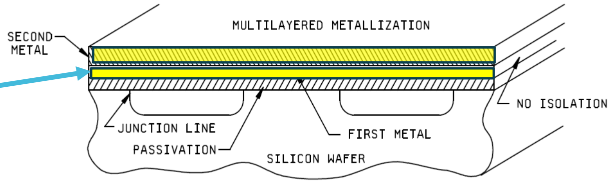


Feature on a MMIC at high mag. Color fringing in the silicon nitride adjacent to via

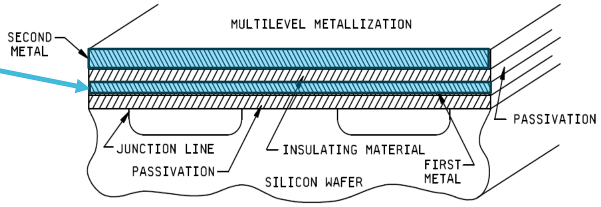
The various colors seen when inspectiong and IC/MMICs are the result of light passing through the oxide (SiO2) or silicon nitride and reflecting back to the optical receiver (aka your eye). There is a relationship between the color viewed and the thickness of this layer. One indication there is a particle buried under the glass is “evidence of color fringing” surrounding the buried particle in the glass layer.

IC Multilayer vs. Multilevel Metal

Multiple layers of metal deposited over each other without isolation



Multiple layers of metallization separated by passivation providing isolation



TM 2010 FIG 2010-3

Course Notes

TM 2010 Requirements as per TM 2017 Table

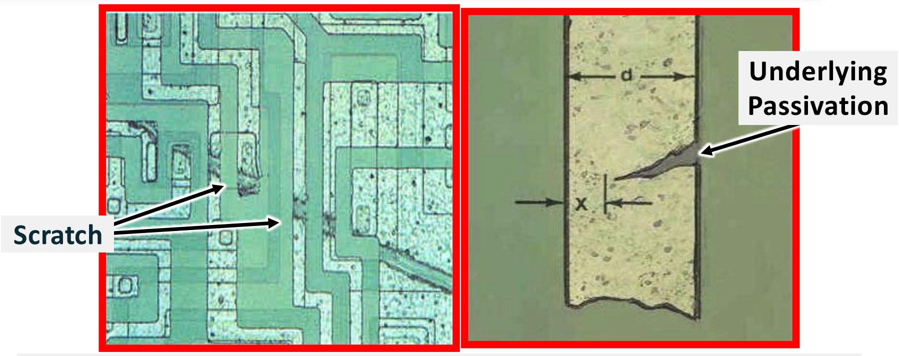
High Magnification

Para. 3.1.1: Metallization defects
  Para. 3.1.1.8 Via Hole Metallization
  Para. 3.1.1.9 MMIC Coupling (air) bridge defects
Para. 3.1.2: Diffusion and passivation layer(s) faults
Para. 3.1.3: Scribing and die defects
Para. 3.1.4: Glassivation defects

NOTE: Die attach and wirebond inspection criteria for Hybrids is contained in TM 2017

Single Layer Metal Scratch Criteria

REJECT



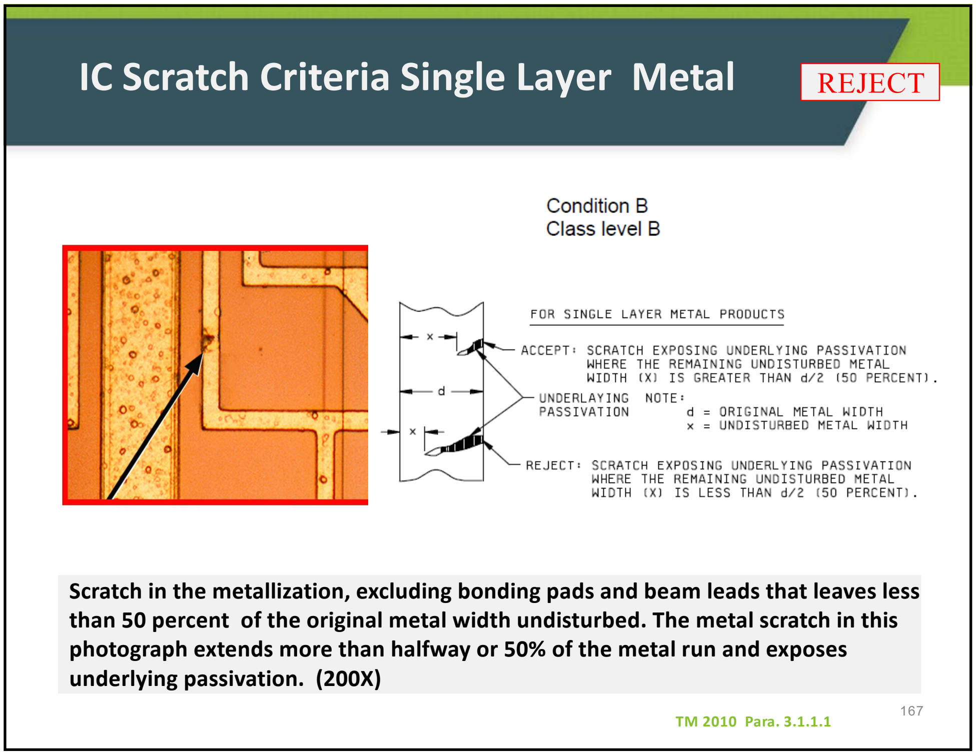
Class B: Scratch that exposes underlying passivation anywhere along its length AND leaves < 50% of the original metal width undisturbed.

Scratch that completely crosses a metallization path and damages the surface of the surrounding passivation, glassivation or substrate.

NOTE: For GaAs microwave devices, scratches in the gate stripe or gate insertion metallization.

TM 2010 Para. 3.1.1.1

Course Notes



IC Scratch Criteria Single Layer Metal

REJECT

Condition B
Class level B

FOR SINGLE LAYER METAL PRODUCTS

ACCEPT: SCRATCH EXPOSING UNDERLYING PASSIVATION WHERE THE REMAINING UNDISTURBED METAL WIDTH (X) IS GREATER THAN d/2 (50 PERCENT).

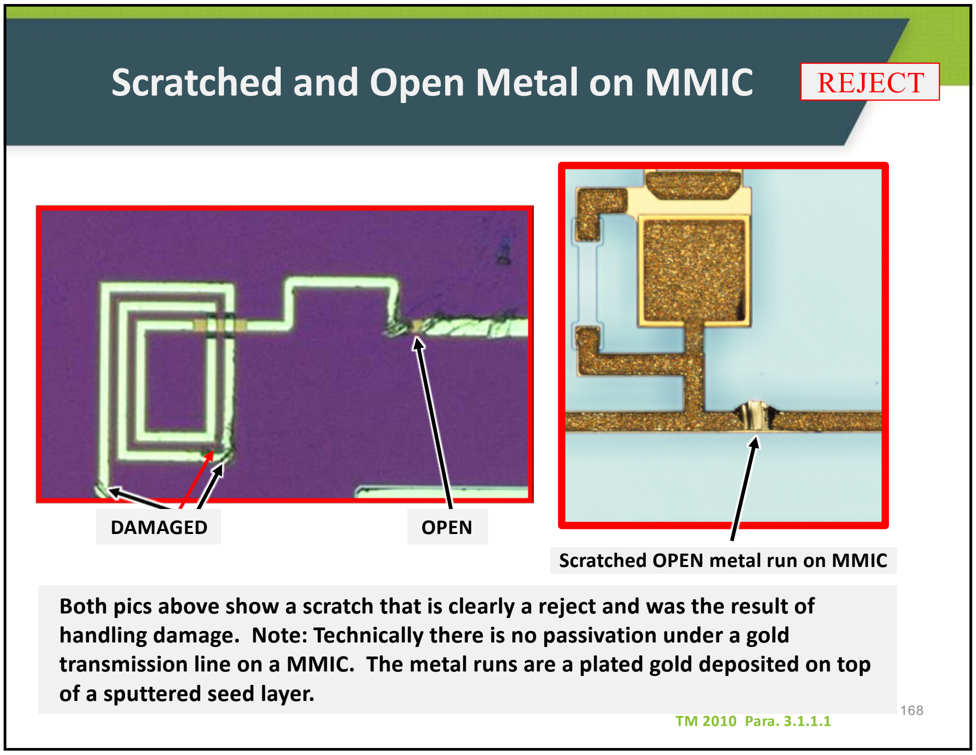
UNDERLAYING PASSIVATION

NOTE:
d = ORIGINAL METAL WIDTH
x = UNDISTURBED METAL WIDTH

REJECT: SCRATCH EXPOSING UNDERLYING PASSIVATION WHERE THE REMAINING UNDISTURBED METAL WIDTH (X) IS LESS THAN d/2 (50 PERCENT).

Scratch in the metallization, excluding bonding pads and beam leads that leaves less than 50 percent of the original metal width undisturbed. The metal scratch in this photograph extends more than halfway or 50% of the metal run and exposes underlying passivation. (200X)

TM 2010 Para. 3.1.1.1



Scratched and Open Metal on MMIC

REJECT

DAMAGED

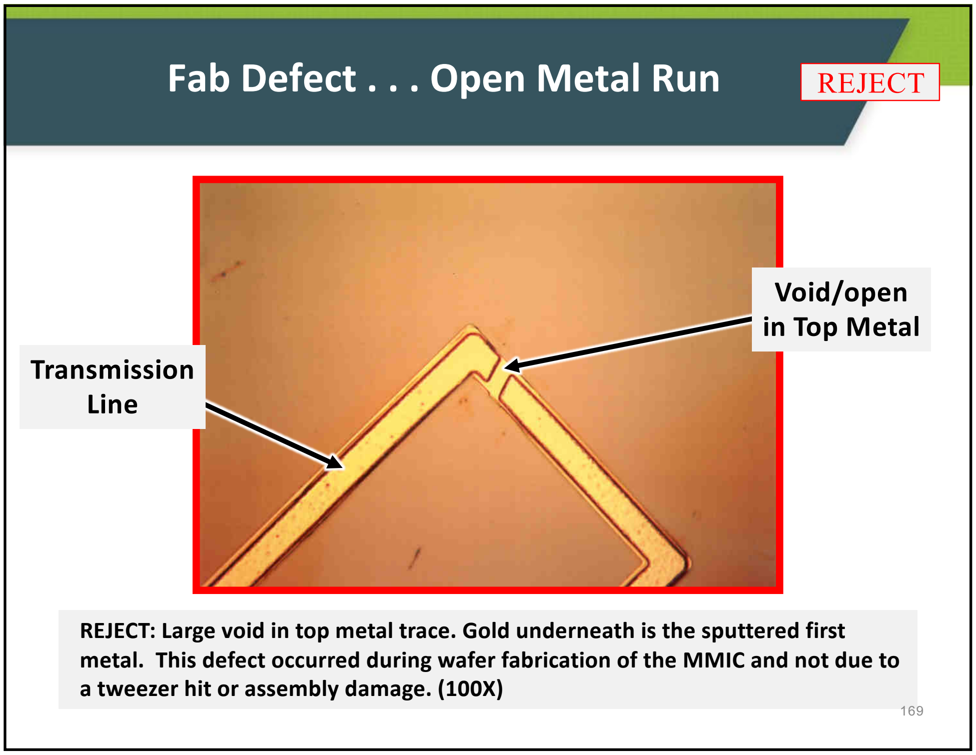
OPEN

Scratched OPEN metal run on MMIC

Both pics above show a scratch that is clearly a reject and was the result of handling damage. Note: Technically there is no passivation under a gold transmission line on a MMIC. The metal runs are a plated gold deposited on top of a sputtered seed layer.

TM 2010 Para. 3.1.1.1

Course Notes



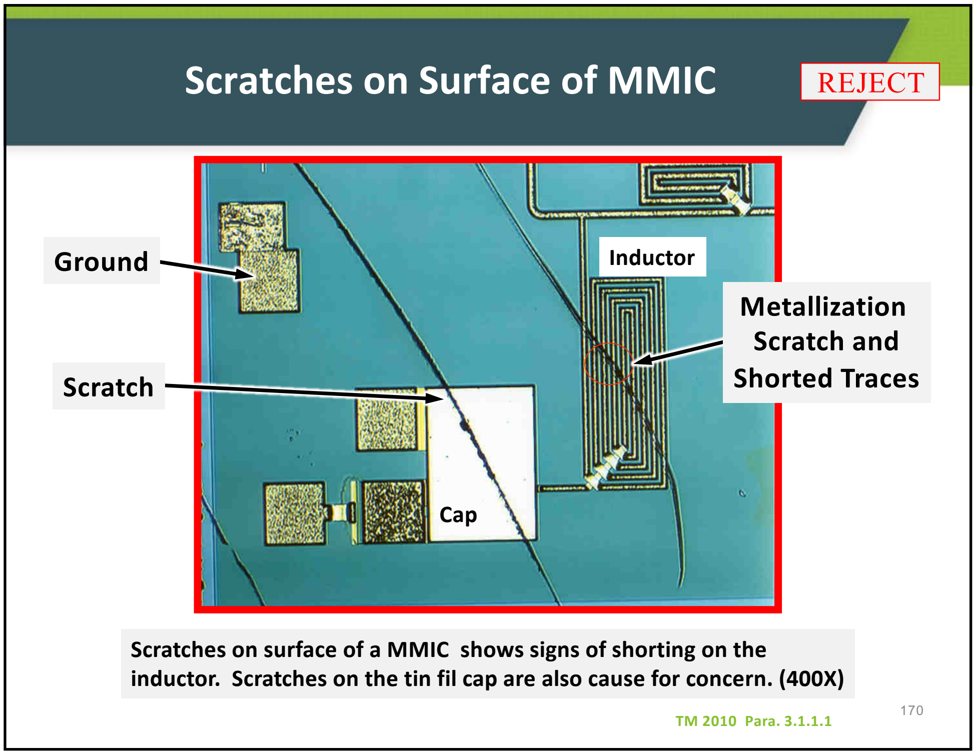
Fab Defect . . . Open Metal Run

REJECT

Void/open in Top Metal

Transmission Line

REJECT: Large void in top metal trace. Gold underneath is the sputtered first metal. This defect occurred during wafer fabrication of the MMIC and not due to a tweezer hit or assembly damage. (100X)



Scratches on Surface of MMIC

REJECT

Ground

Inductor

Metallization Scratch and Shorted Traces

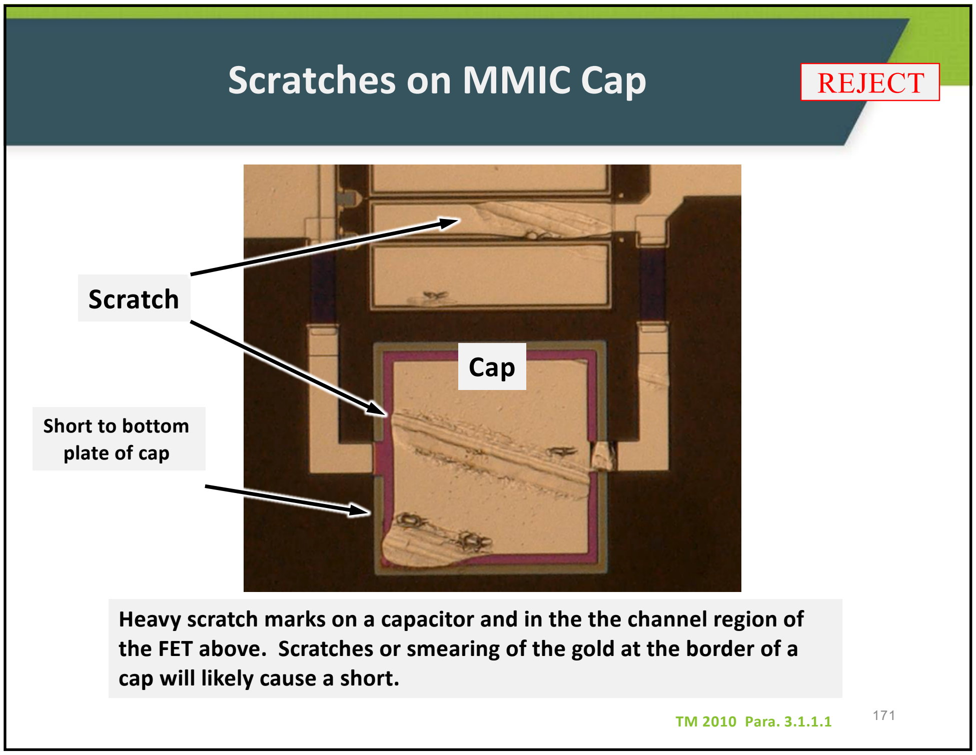
Scratch

Cap

Scratches on surface of a MMIC shows signs of shorting on the inductor. Scratches on the tin fil cap are also cause for concern. (400X)

TM 2010 Para. 3.1.1.1

Course Notes

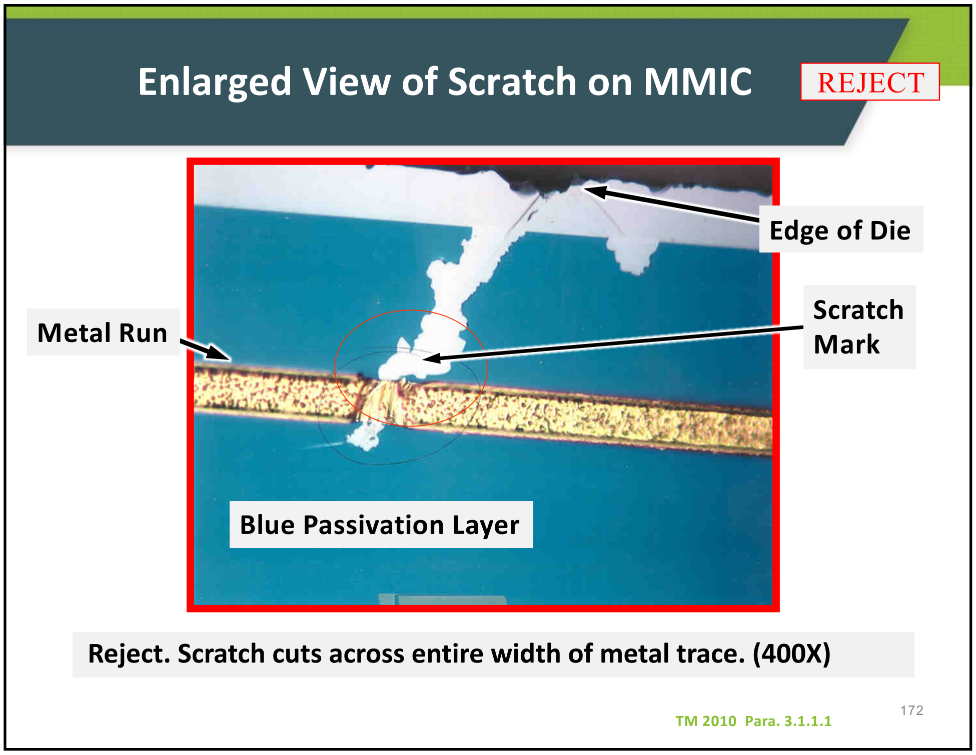


Scratches on MMIC Cap

REJECT

Heavy scratch marks on a capacitor and in the the channel region of the FET above. Scratches or smearing of the gold at the border of a cap will likely cause a short.

TM 2010 Para. 3.1.1.1



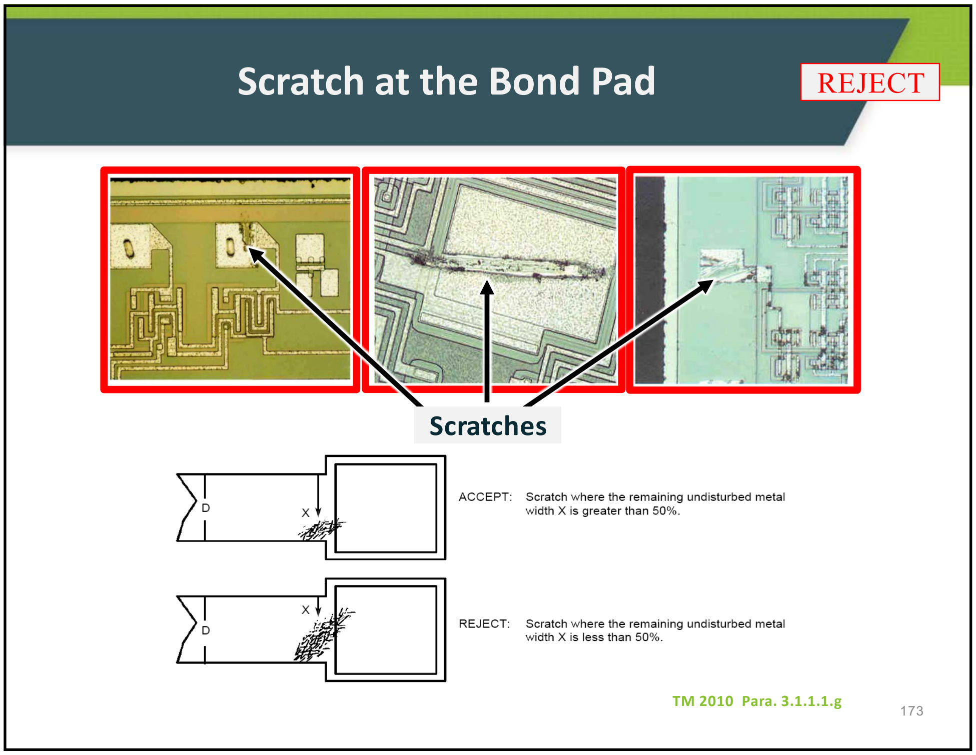
Enlarged View of Scratch on MMIC

REJECT

Reject. Scratch cuts across entire width of metal trace. (400X)

TM 2010 Para. 3.1.1.1

Course Notes



Scratch at the Bond Pad

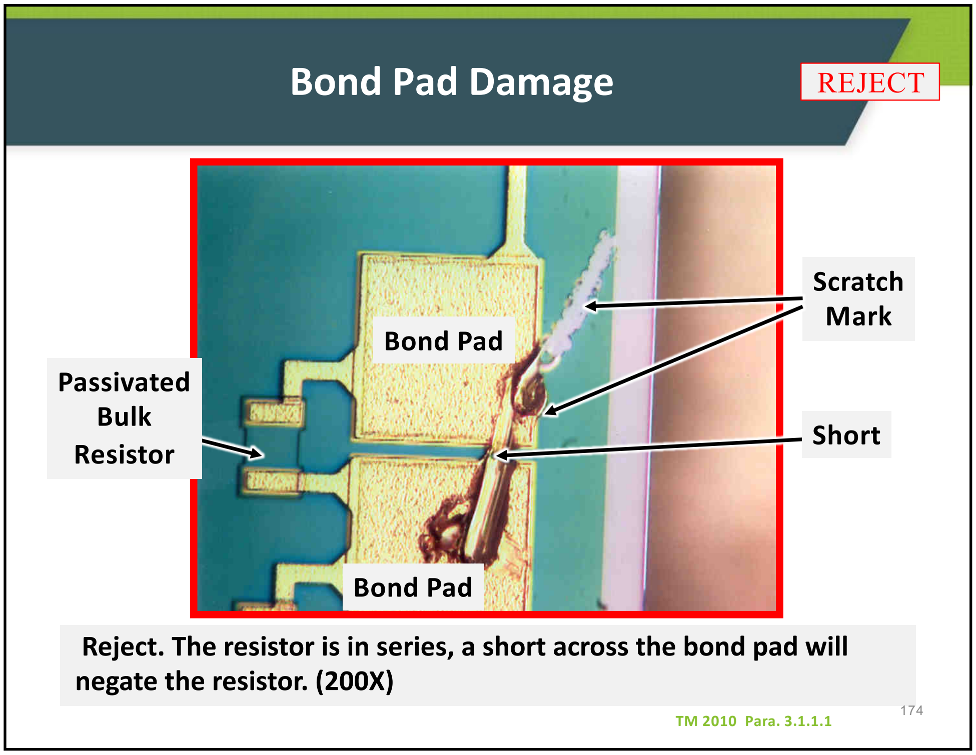
REJECT

Scratches

ACCEPT: Scratch where the remaining undisturbed metal width X is greater than 50%.

REJECT: Scratch where the remaining undisturbed metal width X is less than 50%.

TM 2010 Para. 3.1.1.1.g

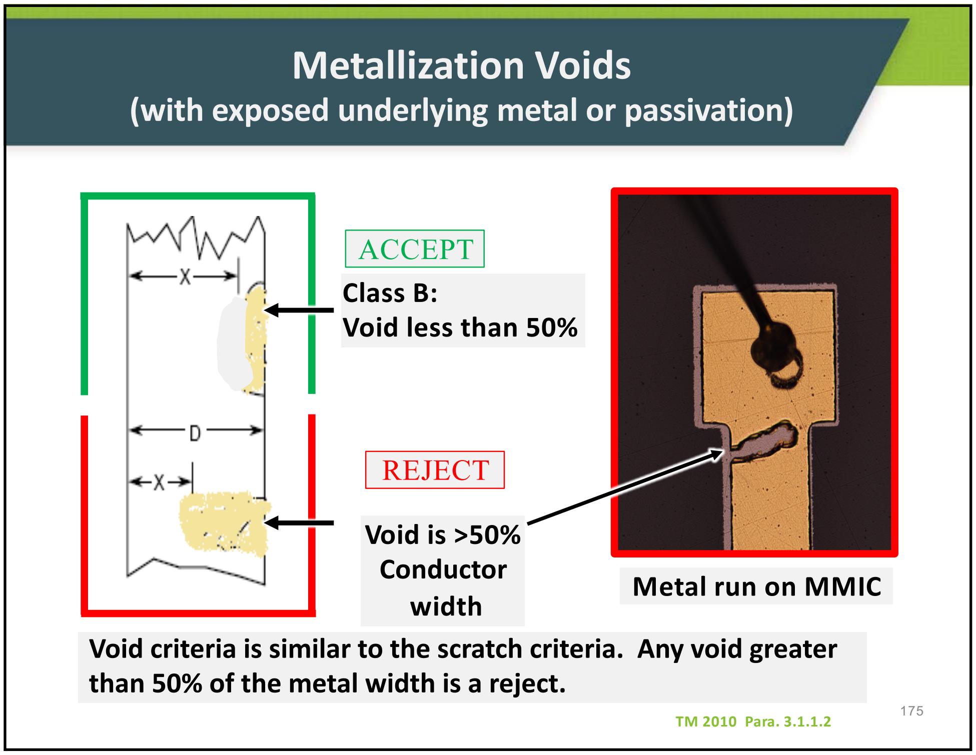


Bond Pad Damage

REJECT

Reject. The resistor is in series, a short across the bond pad will negate the resistor. (200X)

TM 2010 Para. 3.1.1.1



Metallization Voids
(with exposed underlying metal or passivation)

ACCEPT

Class B:
Void less than 50%

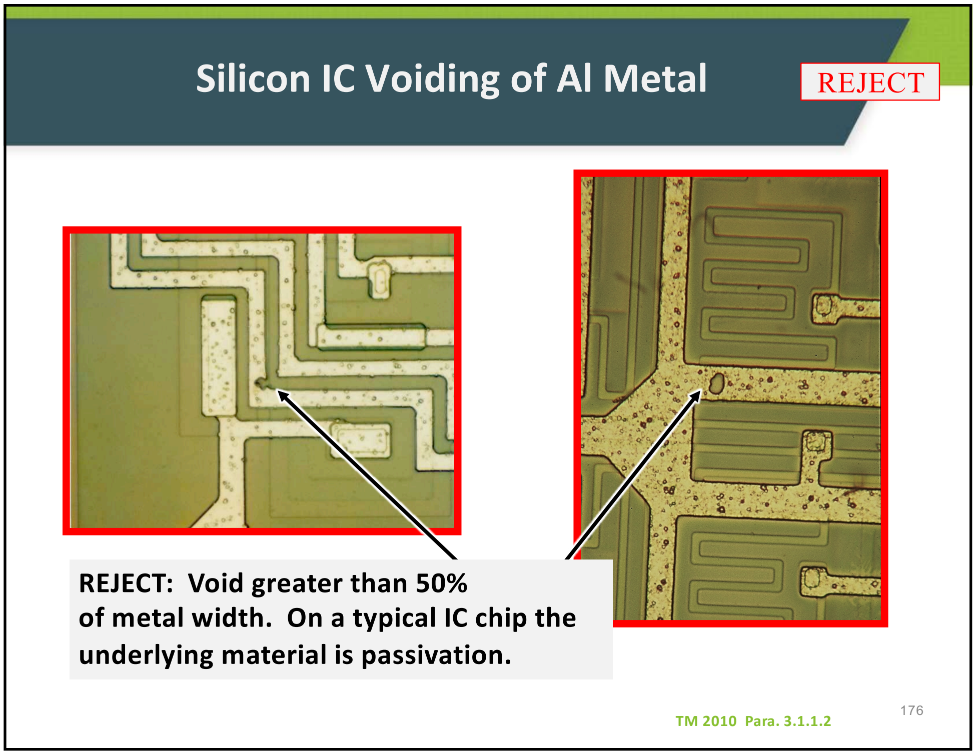
REJECT

Void is >50% Conductor width

Metal run on MMIC

Void criteria is similar to the scratch criteria. Any void greater than 50% of the metal width is a reject.

TM 2010 Para. 3.1.1.2

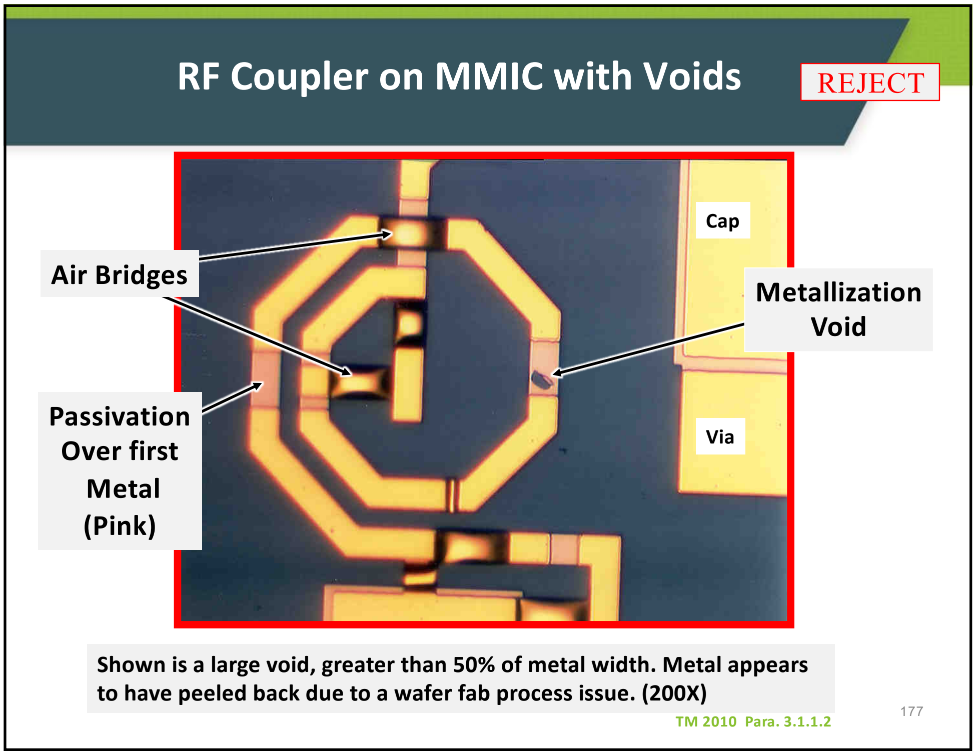


Silicon IC Voiding of Al Metal

REJECT

REJECT: Void greater than 50% of metal width. On a typical IC chip the underlying material is passivation.

TM 2010 Para. 3.1.1.2



RF Coupler on MMIC with Voids

REJECT

Air Bridges

Passivation Over first Metal (Pink)

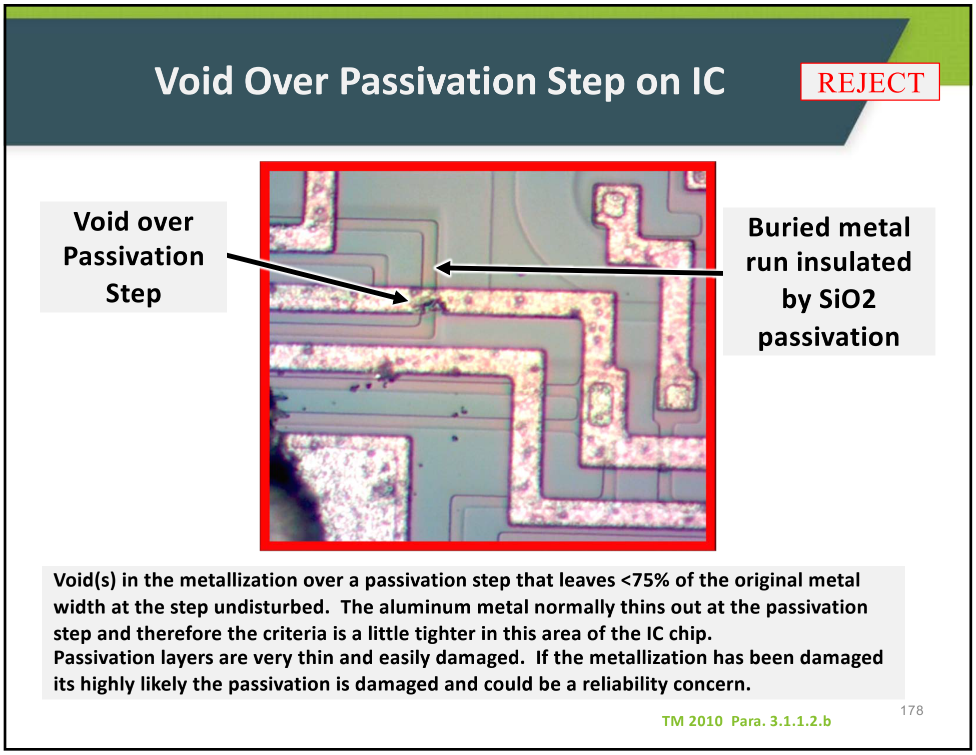
Cap

Metallization Void

Via

Shown is a large void, greater than 50% of metal width. Metal appears to have peeled back due to a wafer fab process issue. (200X)

TM 2010 Para. 3.1.1.2



Void Over Passivation Step on IC

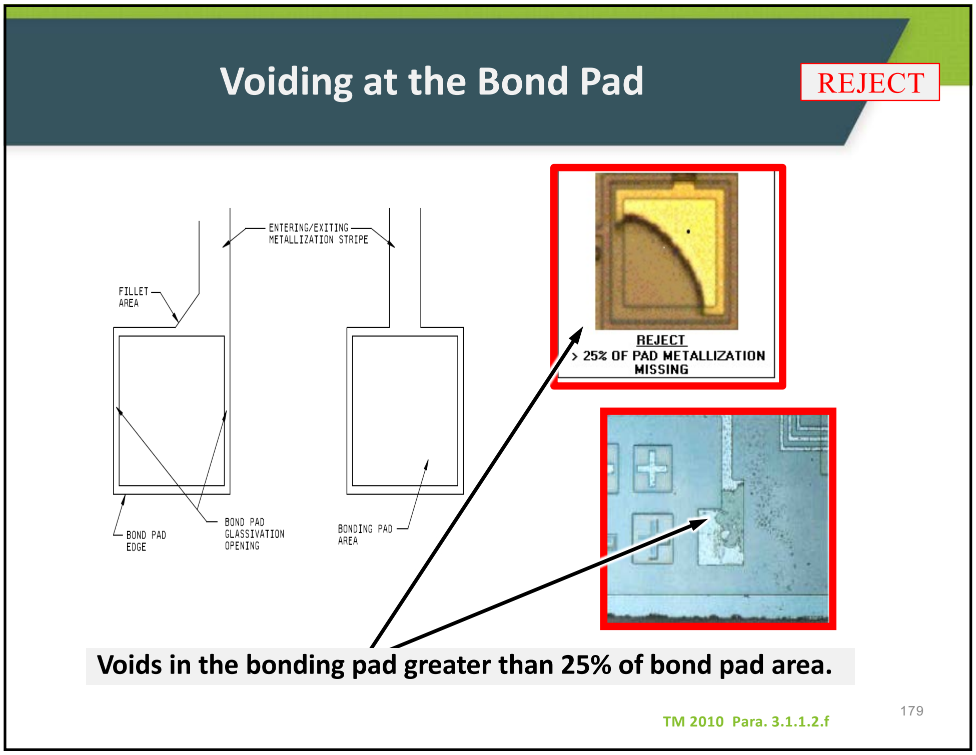
REJECT

Void over Passivation Step

Buried metal run insulated by SiO2 passivation

Void(s) in the metallization over a passivation step that leaves <75% of the original metal width at the step undisturbed. The aluminum metal normally thins out at the passivation step and therefore the criteria is a little tighter in this area of the IC chip.
Passivation layers are very thin and easily damaged. If the metallization has been damaged its highly likely the passivation is damaged and could be a reliability concern.

TM 2010 Para. 3.1.1.2.b

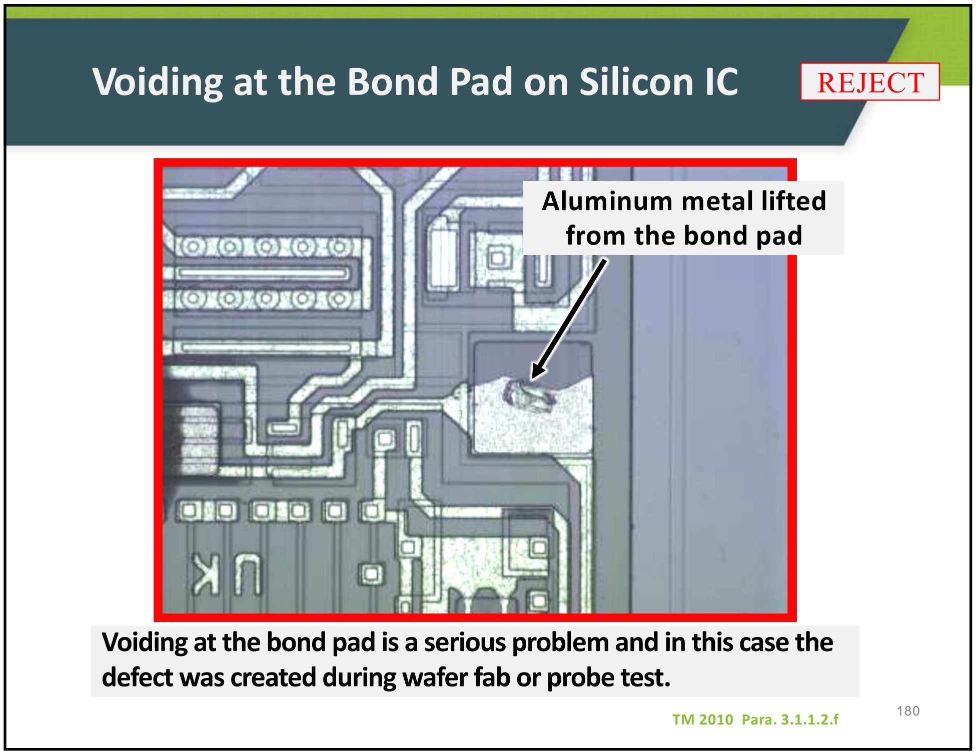


Voiding at the Bond Pad

REJECT

Voids in the bonding pad greater than 25% of bond pad area.

TM 2010 Para. 3.1.1.2.f



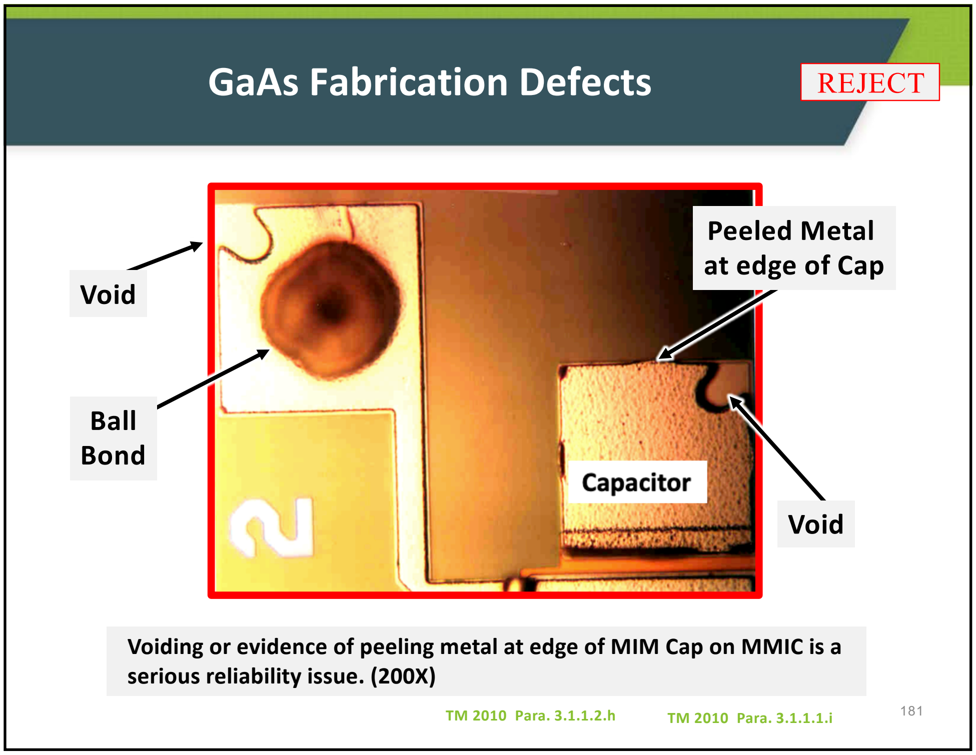
Voiding at the Bond Pad on Silicon IC

REJECT

Aluminum metal lifted from the bond pad

Voiding at the bond pad is a serious problem and in this case the defect was created during wafer fab or probe test.

TM 2010 Para. 3.1.1.2.f

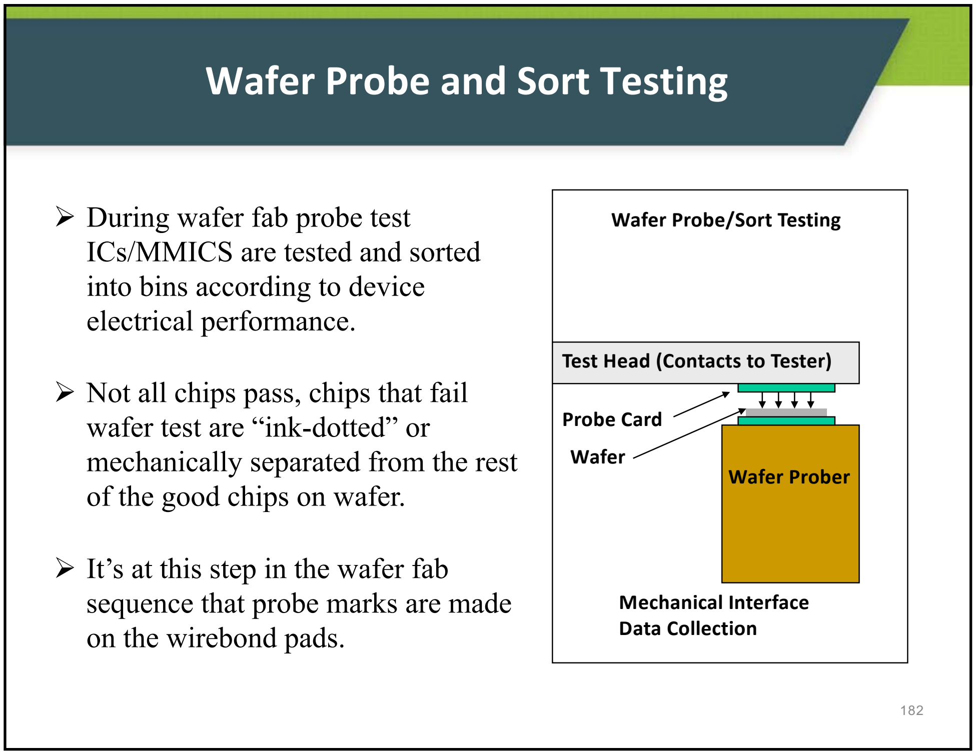


GaAs Fabrication Defects

REJECT

Voiding or evidence of peeling metal at edge of MIM Cap on MMIC is a serious reliability issue. (200X)

TM 2010 Para. 3.1.1.2.h TM 2010 Para. 3.1.1.1.i

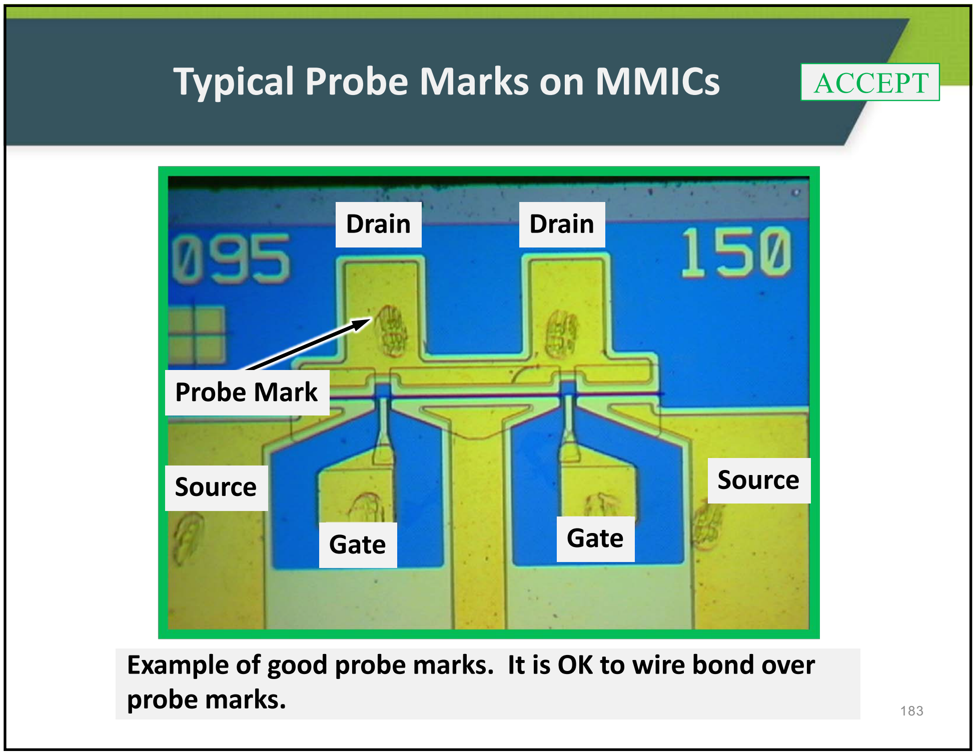


Wafer Probe and Sort Testing

- During wafer fab probe test ICs/MMICS are tested and sorted into bins according to device electrical performance.
- Not all chips pass, chips that fail wafer test are “ink-dotted” or mechanically separated from the rest of the good chips on wafer.
- It’s at this step in the wafer fab sequence that probe marks are made on the wirebond pads.

Wafer Probe/Sort Testing

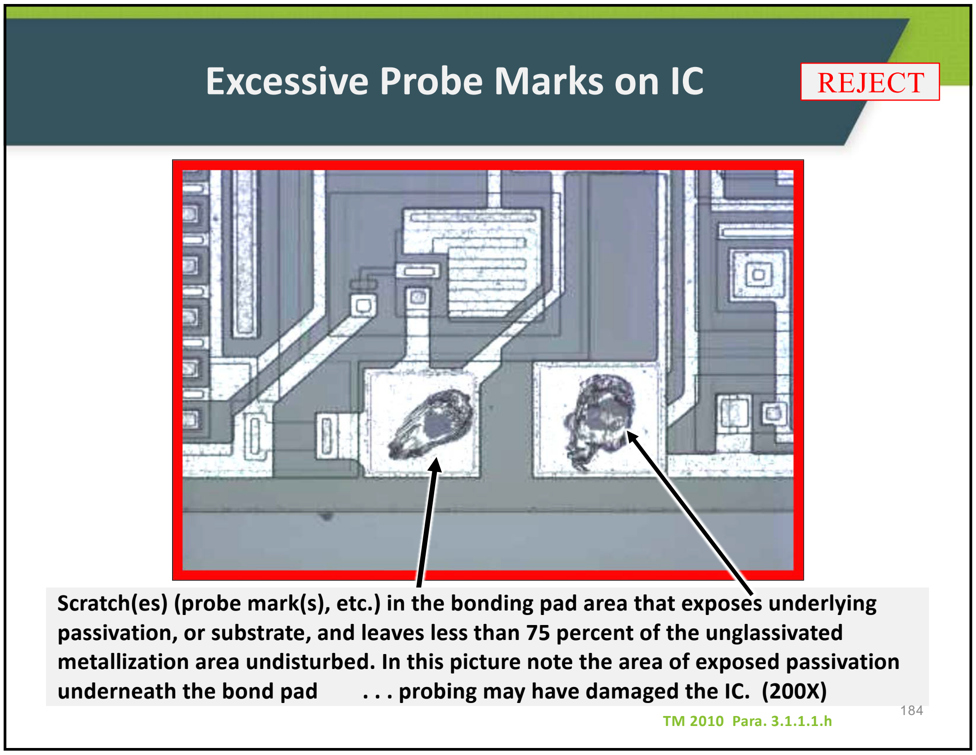
Course Notes



Typical Probe Marks on MMICs

ACCEPT

Example of good probe marks. It is OK to wire bond over probe marks.



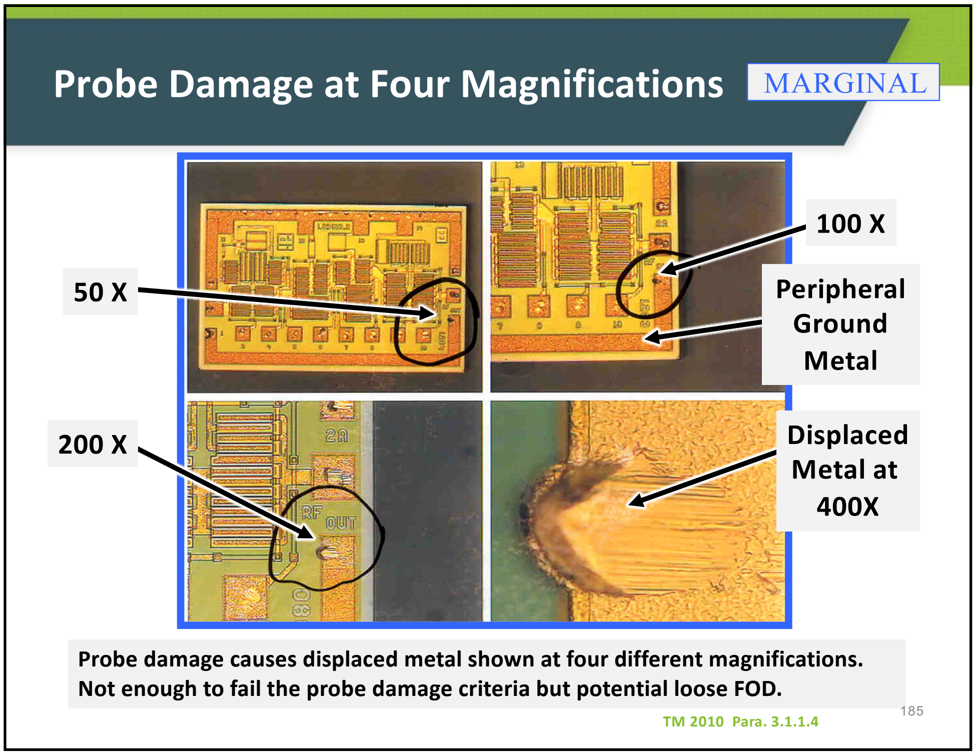
Excessive Probe Marks on IC

REJECT

Scratch(es) (probe mark(s), etc.) in the bonding pad area that exposes underlying passivation, or substrate, and leaves less than 75 percent of the unglassivated metallization area undisturbed. In this picture note the area of exposed passivation underneath the bond pad . . . probing may have damaged the IC. (200X)

TM 2010 Para. 3.1.1.1.h

Course Notes



Probe Damage at Four Magnifications

MARGINAL

50 X

100 X

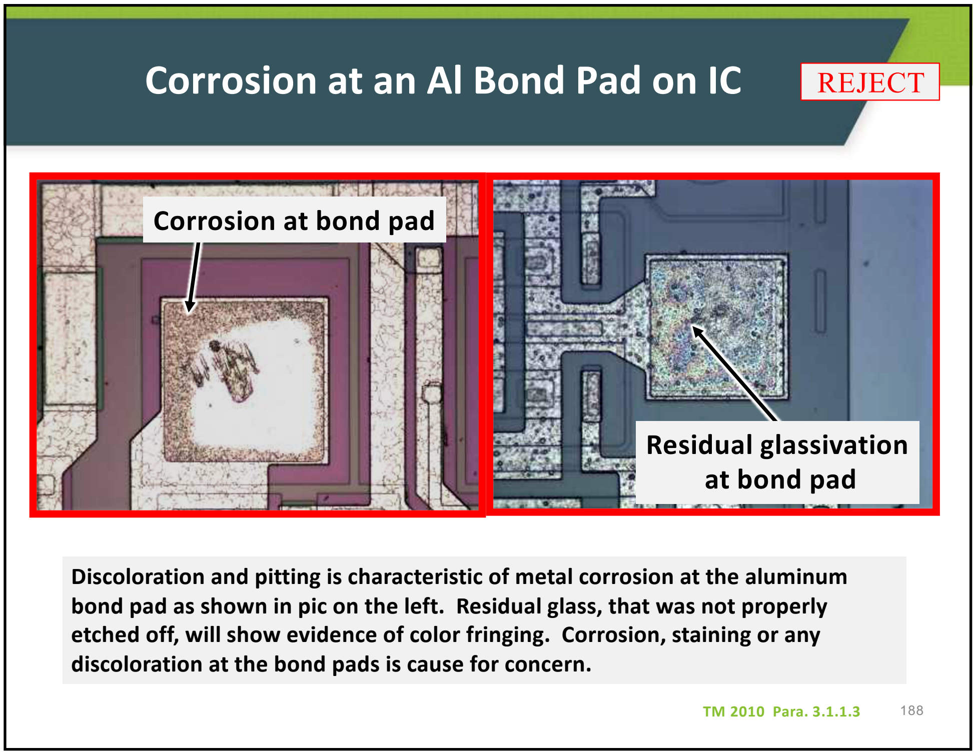
Peripheral Ground Metal

200 X

Displaced Metal at 400X

Probe damage causes displaced metal shown at four different magnifications. Not enough to fail the probe damage criteria but potential loose FOD.

TM 2010 Para. 3.1.1.4



Corrosion at an Al Bond Pad on IC

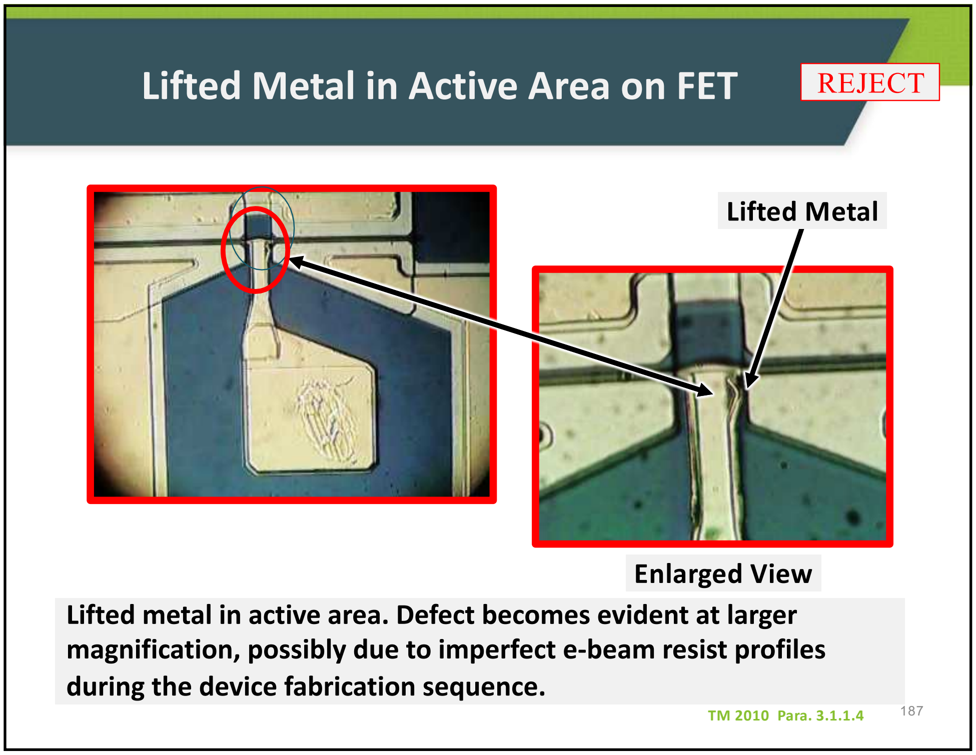
REJECT

Corrosion at bond pad

Residual glassivation at bond pad

Discoloration and pitting is characteristic of metal corrosion at the aluminum bond pad as shown in pic on the left. Residual glass, that was not properly etched off, will show evidence of color fringing. Corrosion, staining or any discoloration at the bond pads is cause for concern.

TM 2010 Para. 3.1.1.3

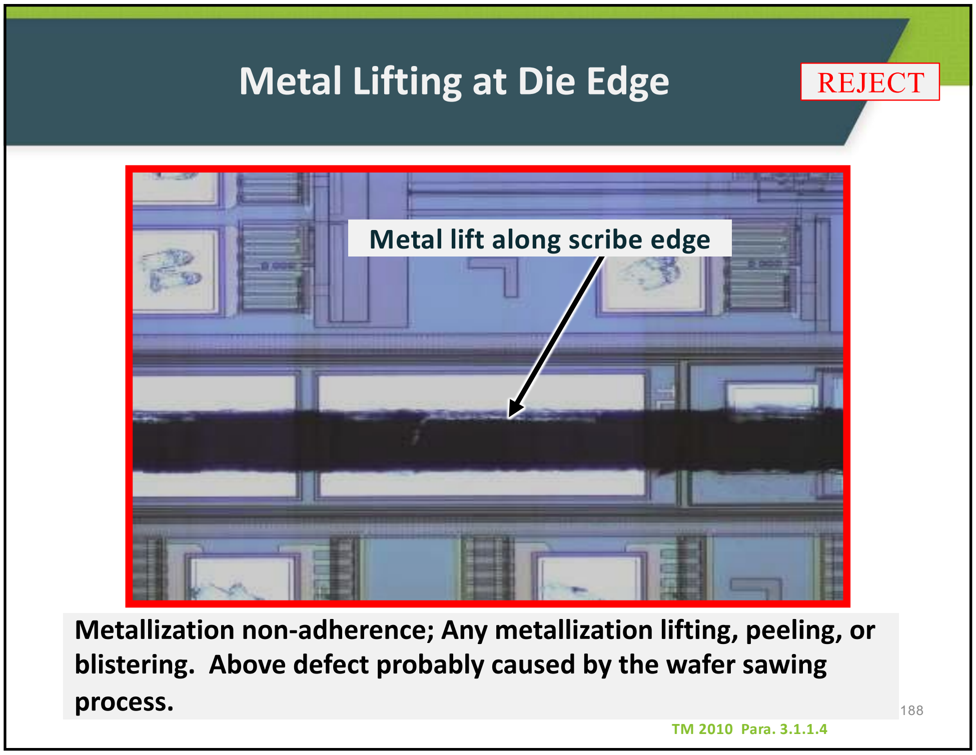


Lifted Metal in Active Area on FET

REJECT

Lifted metal in active area. Defect becomes evident at larger magnification, possibly due to imperfect e-beam resist profiles during the device fabrication sequence.

TM 2010 Para. 3.1.1.4



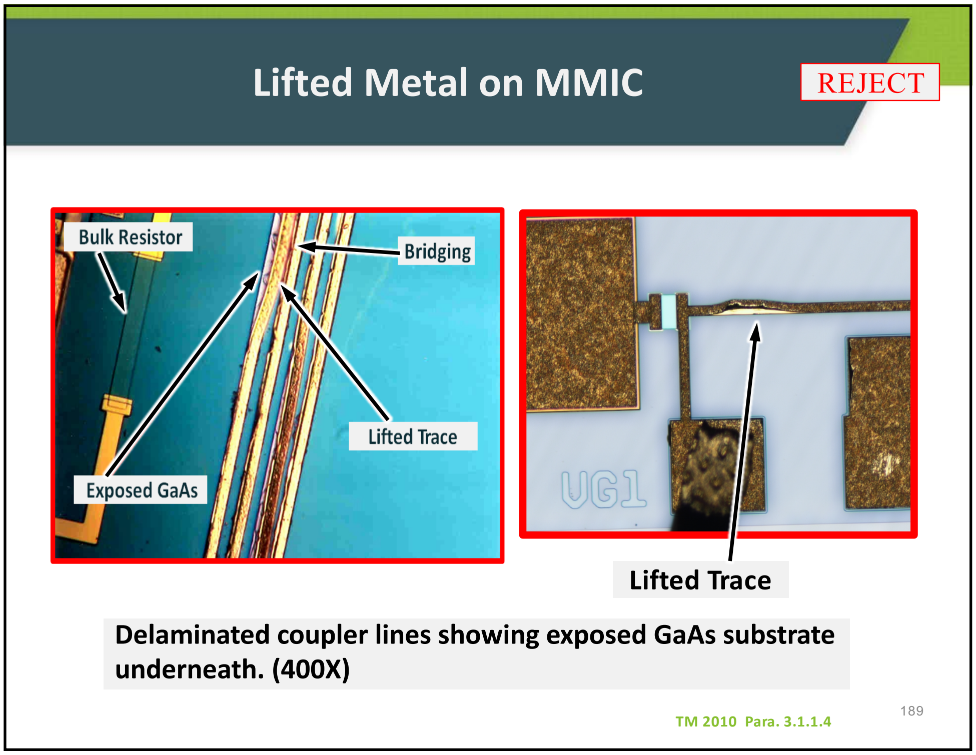
Metal Lifting at Die Edge

REJECT

Metallization non-adherence; Any metallization lifting, peeling, or blistering. Above defect probably caused by the wafer sawing process.

TM 2010 Para. 3.1.1.4

Course Notes

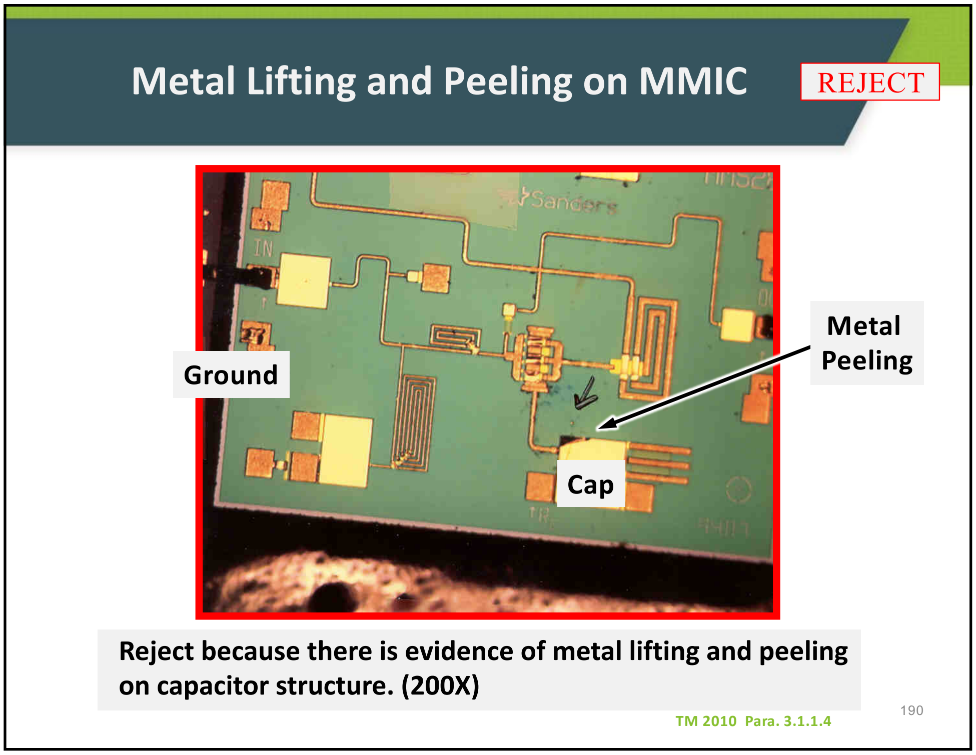


Lifted Metal on MMIC

REJECT

Delaminated coupler lines showing exposed GaAs substrate underneath. (400X)

TM 2010 Para. 3.1.1.4



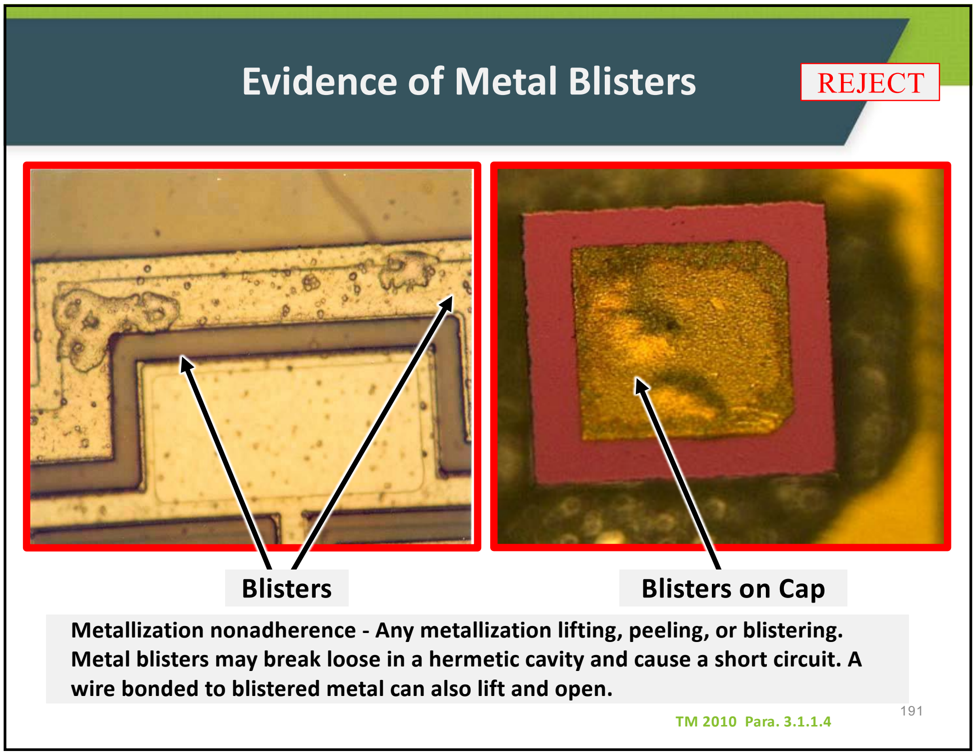
Metal Lifting and Peeling on MMIC

REJECT

Reject because there is evidence of metal lifting and peeling on capacitor structure. (200X)

TM 2010 Para. 3.1.1.4

Course Notes



Evidence of Metal Blisters

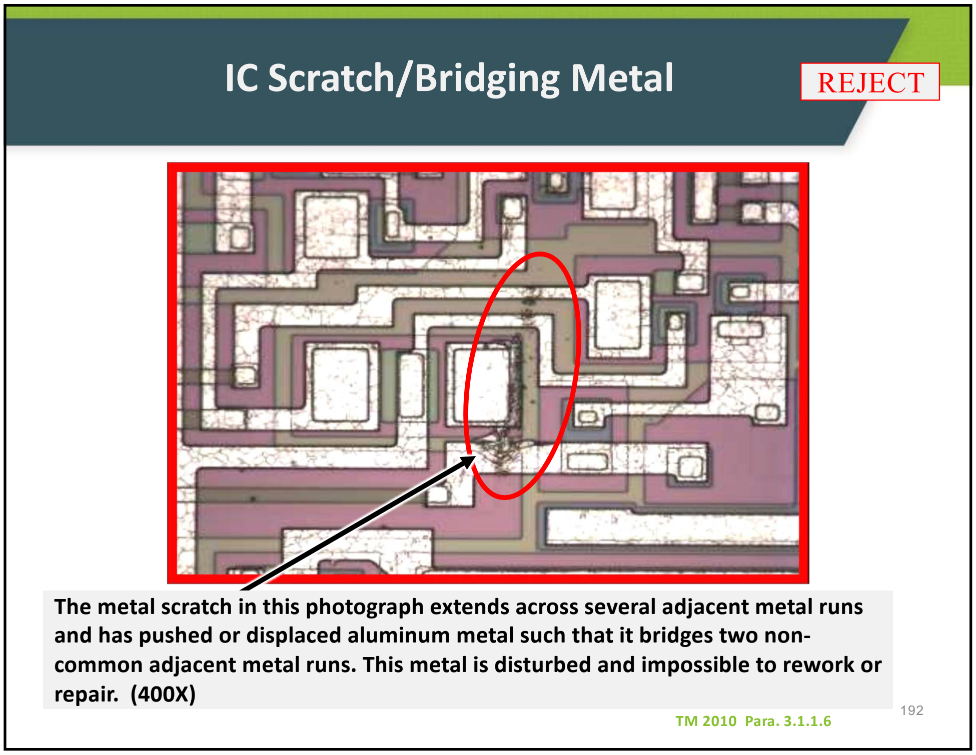
REJECT

Blisters

Blisters on Cap

Metallization nonadherence - Any metallization lifting, peeling, or blistering. Metal blisters may break loose in a hermetic cavity and cause a short circuit. A wire bonded to blistered metal can also lift and open.

TM 2010 Para. 3.1.1.4

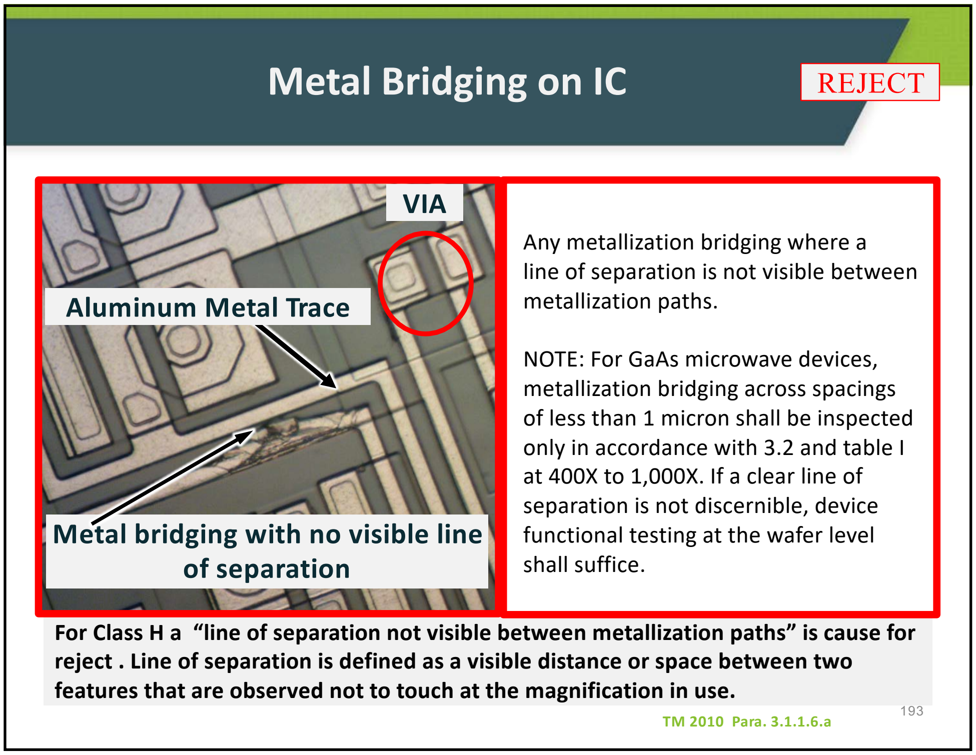


IC Scratch/Bridging Metal

REJECT

The metal scratch in this photograph extends across several adjacent metal runs and has pushed or displaced aluminum metal such that it bridges two non-common adjacent metal runs. This metal is disturbed and impossible to rework or repair. (400X)

TM 2010 Para. 3.1.1.6



Metal Bridging on IC

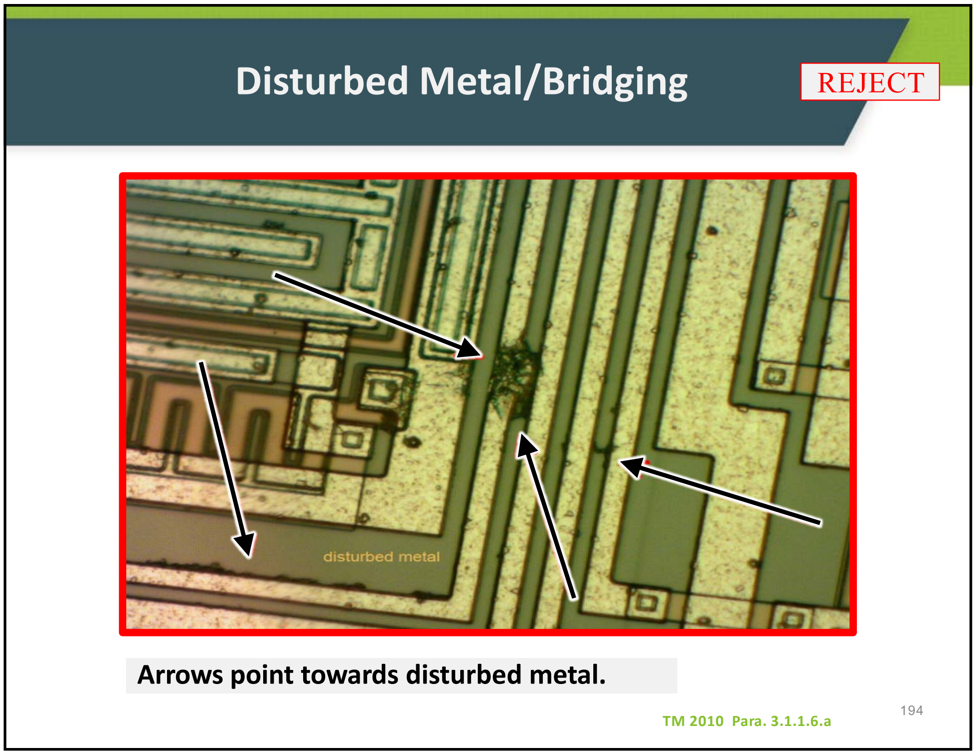
REJECT

Any metallization bridging where a line of separation is not visible between metallization paths.

NOTE: For GaAs microwave devices, metallization bridging across spacings of less than 1 micron shall be inspected only in accordance with 3.2 and table I at 400X to 1,000X. If a clear line of separation is not discernible, device functional testing at the wafer level shall suffice.

For Class H a "line of separation not visible between metallization paths" is cause for reject . Line of separation is defined as a visible distance or space between two features that are observed not to touch at the magnification in use.

TM 2010 Para. 3.1.1.6.a



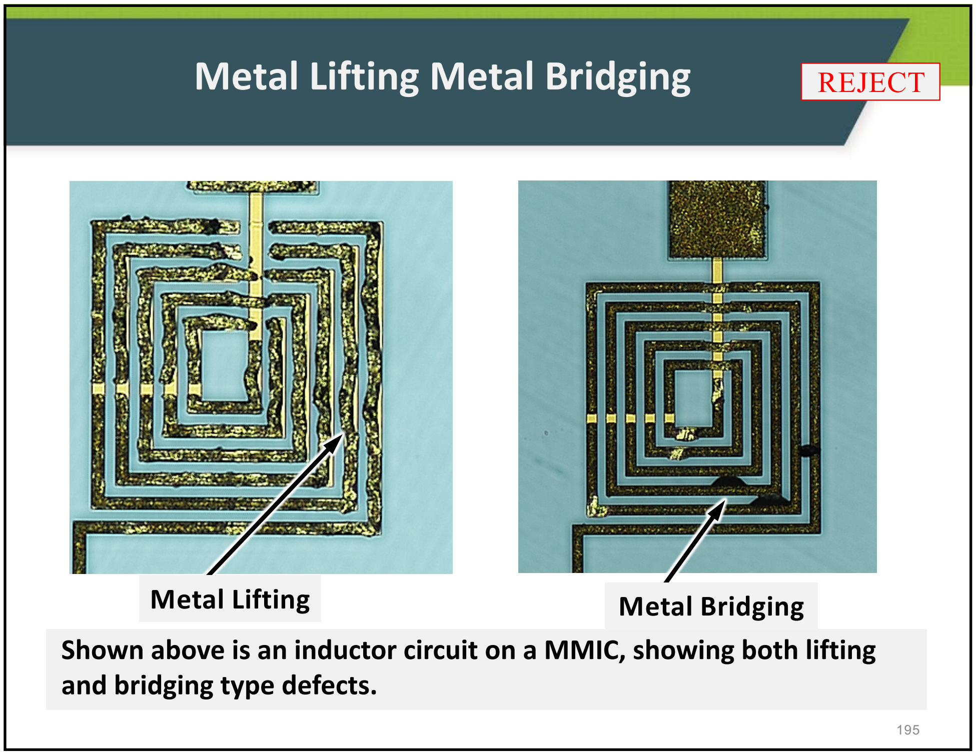
Disturbed Metal/Bridging

REJECT

Arrows point towards disturbed metal.

TM 2010 Para. 3.1.1.6.a

Course Notes



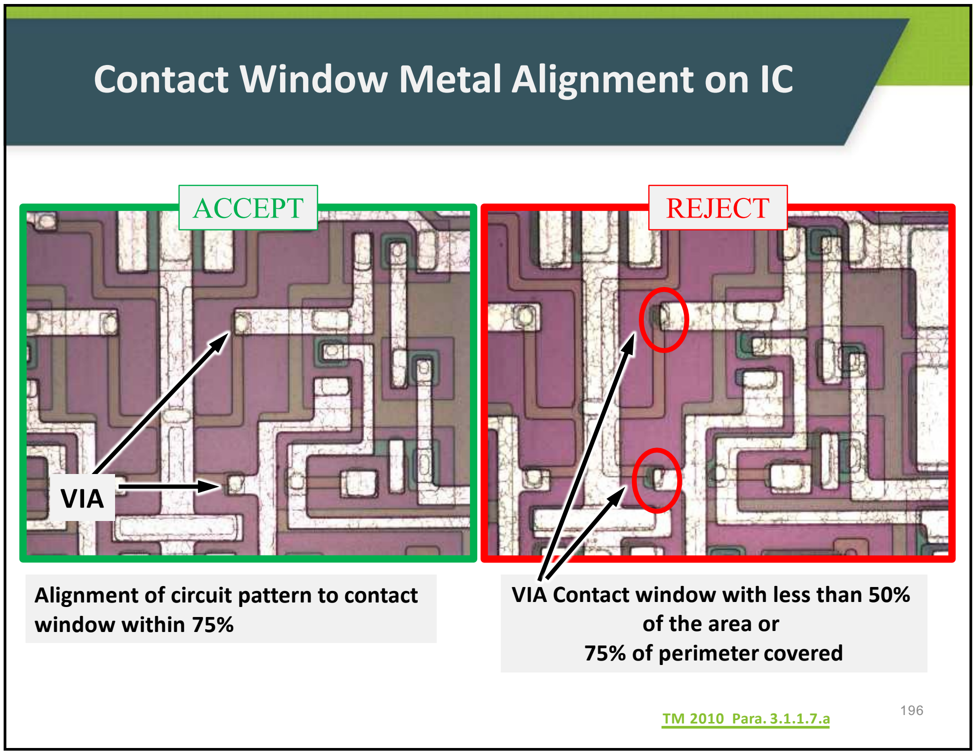
Metal Lifting Metal Bridging

REJECT

Metal Lifting

Metal Bridging

Shown above is an inductor circuit on a MMIC, showing both lifting and bridging type defects.



Contact Window Metal Alignment on IC

ACCEPT

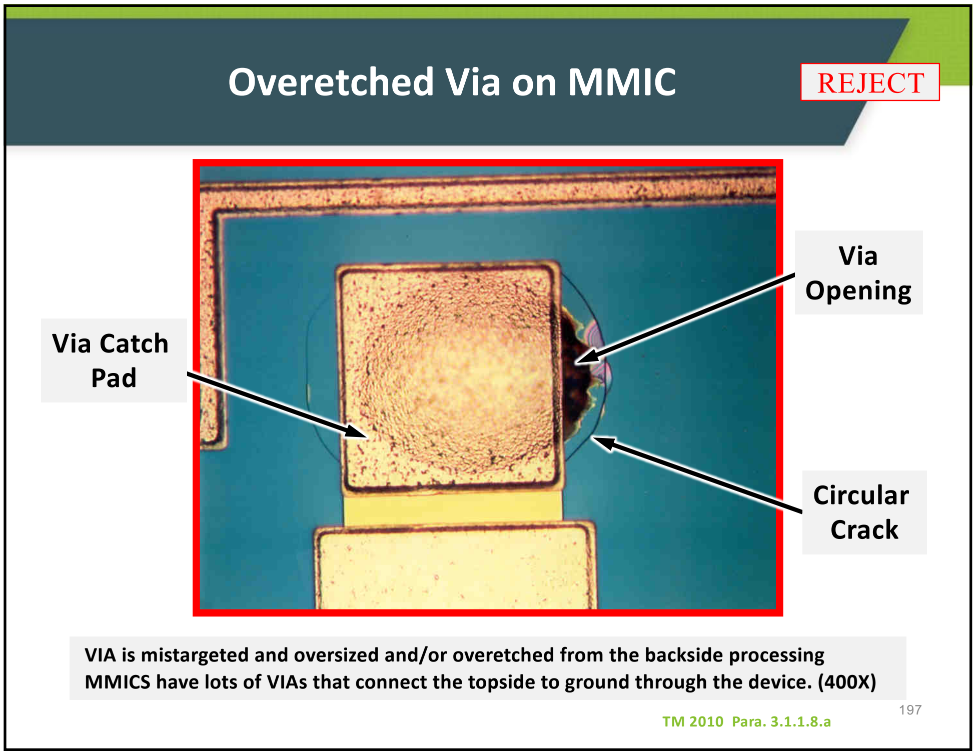
REJECT

VIA

Alignment of circuit pattern to contact window within 75%

VIA Contact window with less than 50%
of the area or
75% of perimeter covered

TM 2010 Para. 3.1.1.7.a

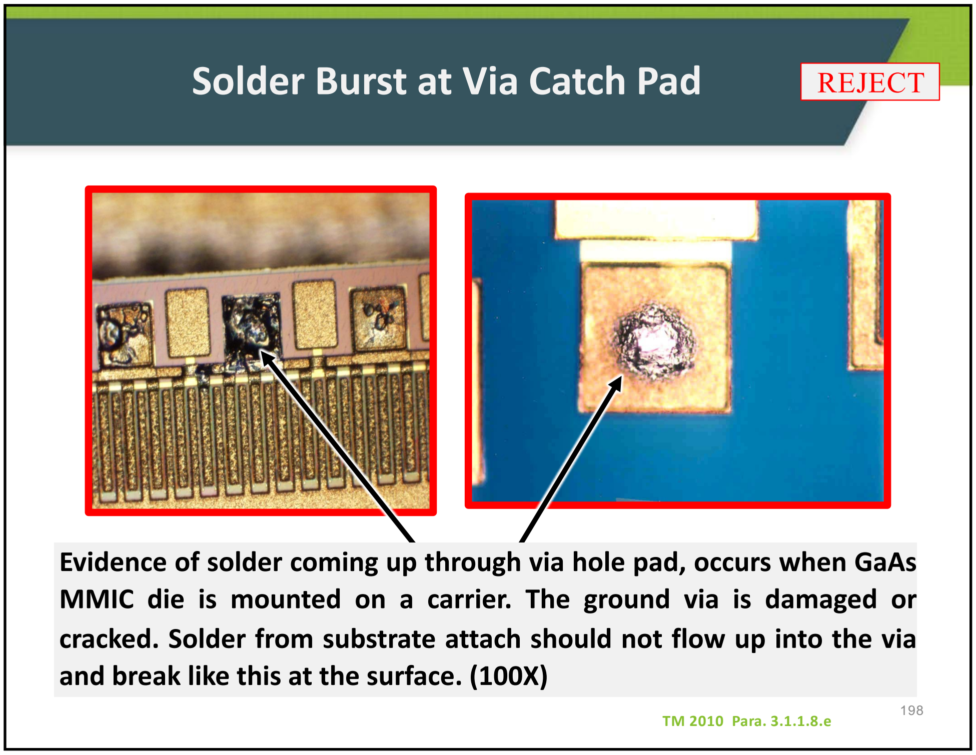


Overetched Via on MMIC

REJECT

VIA is mistargeted and oversized and/or overetched from the backside processing MMICS have lots of VIAs that connect the topside to ground through the device. (400X)

TM 2010 Para. 3.1.1.8.a

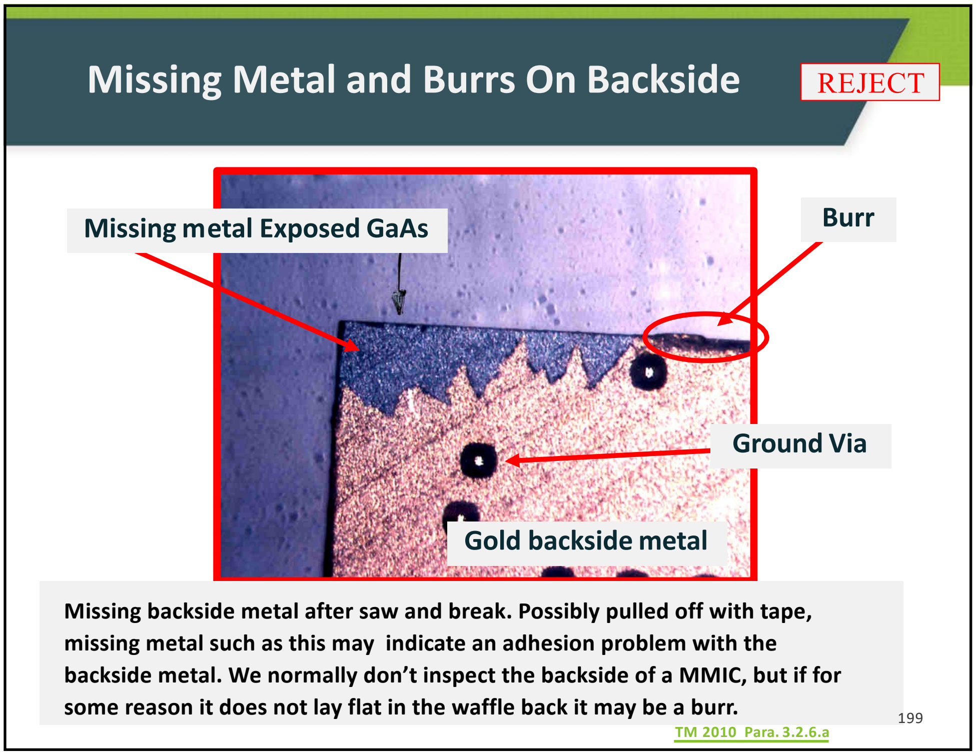


Solder Burst at Via Catch Pad

REJECT

Evidence of solder coming up through via hole pad, occurs when GaAs MMIC die is mounted on a carrier. The ground via is damaged or cracked. Solder from substrate attach should not flow up into the via and break like this at the surface. (100X)

TM 2010 Para. 3.1.1.8.e



Missing Metal and Burrs On Backside

REJECT

Missing metal Exposed GaAs

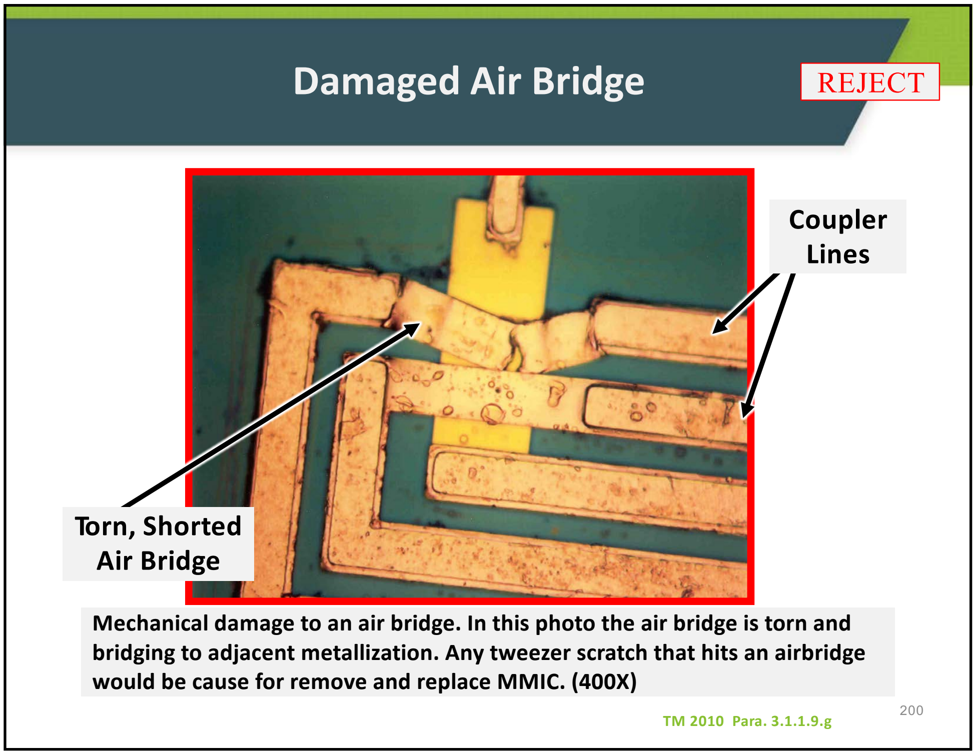
Burr

Ground Via

Gold backside metal

Missing backside metal after saw and break. Possibly pulled off with tape, missing metal such as this may indicate an adhesion problem with the backside metal. We normally don't inspect the backside of a MMIC, but if for some reason it does not lay flat in the waffle back it may be a burr.

TM 2010 Para. 3.2.6.a



Damaged Air Bridge

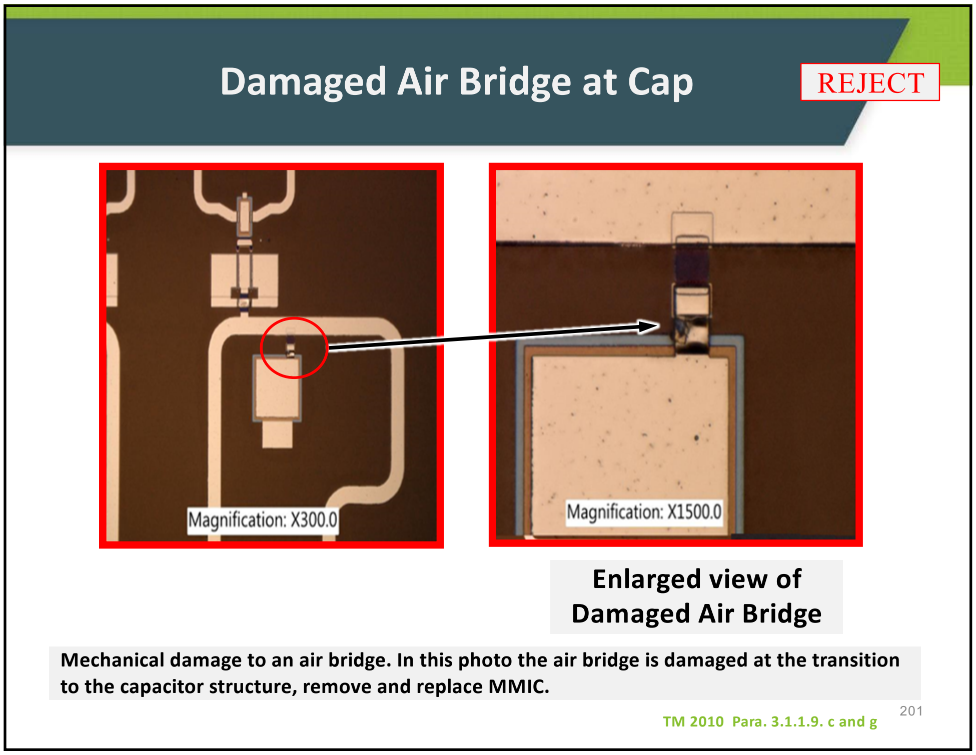
REJECT

Coupler Lines

Torn, Shorted Air Bridge

Mechanical damage to an air bridge. In this photo the air bridge is torn and bridging to adjacent metallization. Any tweezer scratch that hits an airbridge would be cause for remove and replace MMIC. (400X)

TM 2010 Para. 3.1.1.9.g



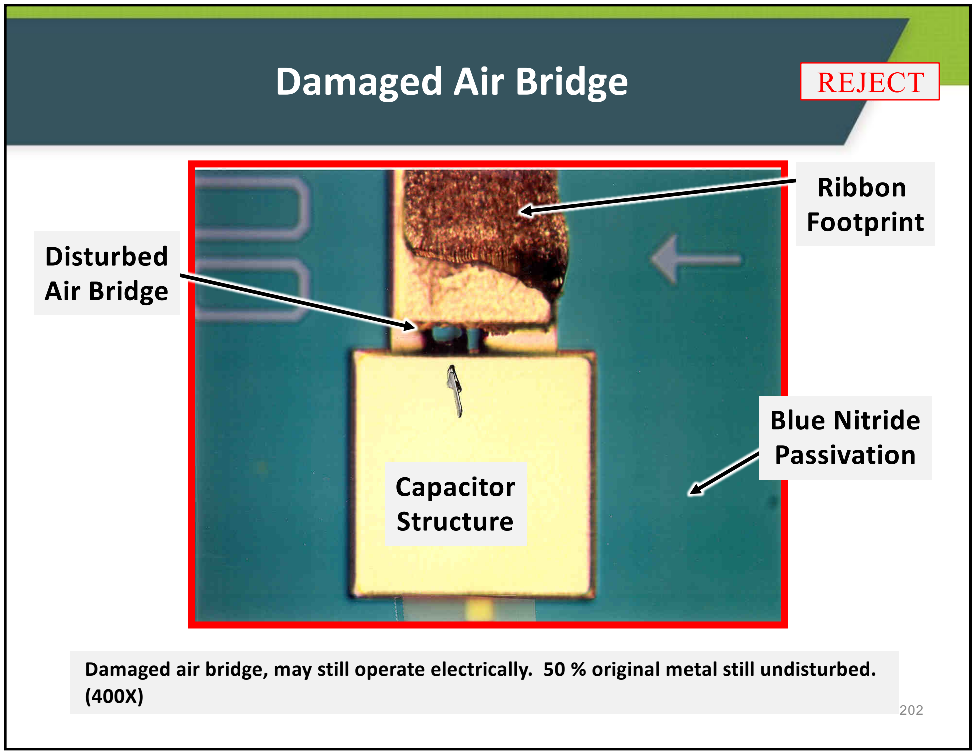
Damaged Air Bridge at Cap

REJECT

Enlarged view of Damaged Air Bridge

Mechanical damage to an air bridge. In this photo the air bridge is damaged at the transition to the capacitor structure, remove and replace MMIC.

TM 2010 Para. 3.1.1.9. c and g



Damaged Air Bridge

REJECT

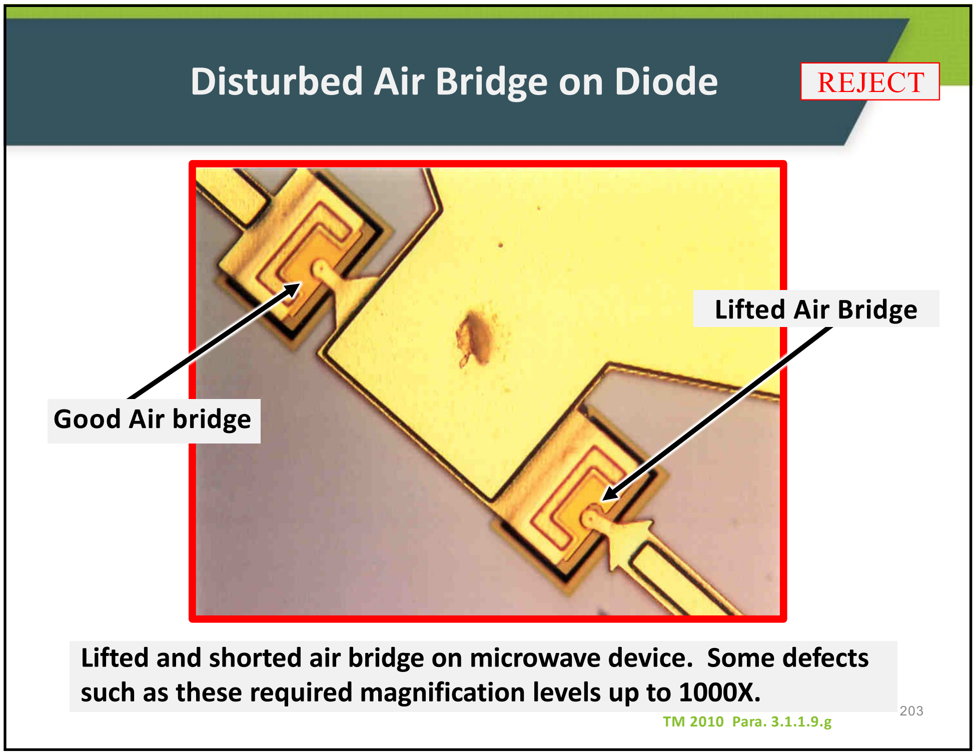
Disturbed Air Bridge

Ribbon Footprint

Blue Nitride Passivation

Capacitor Structure

Damaged air bridge, may still operate electrically. 50 % original metal still undisturbed. (400X)



Disturbed Air Bridge on Diode

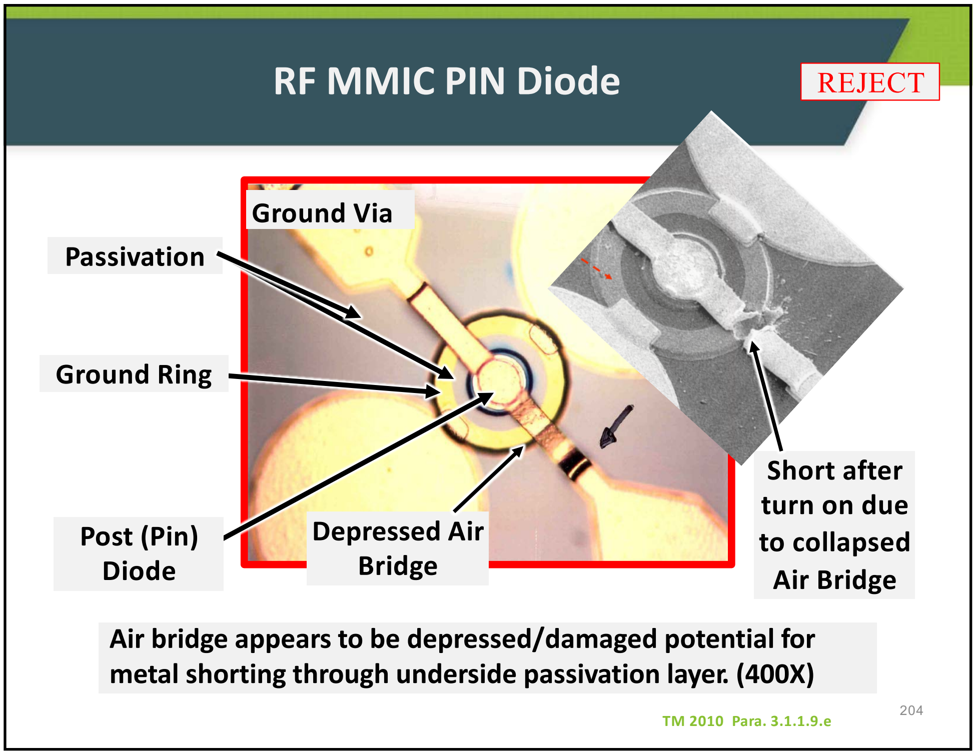
REJECT

Good Air bridge

Lifted Air Bridge

Lifted and shorted air bridge on microwave device. Some defects such as these required magnification levels up to 1000X.

TM 2010 Para. 3.1.1.9.g



RF MMIC PIN Diode

REJECT

Ground Via

Passivation

Ground Ring

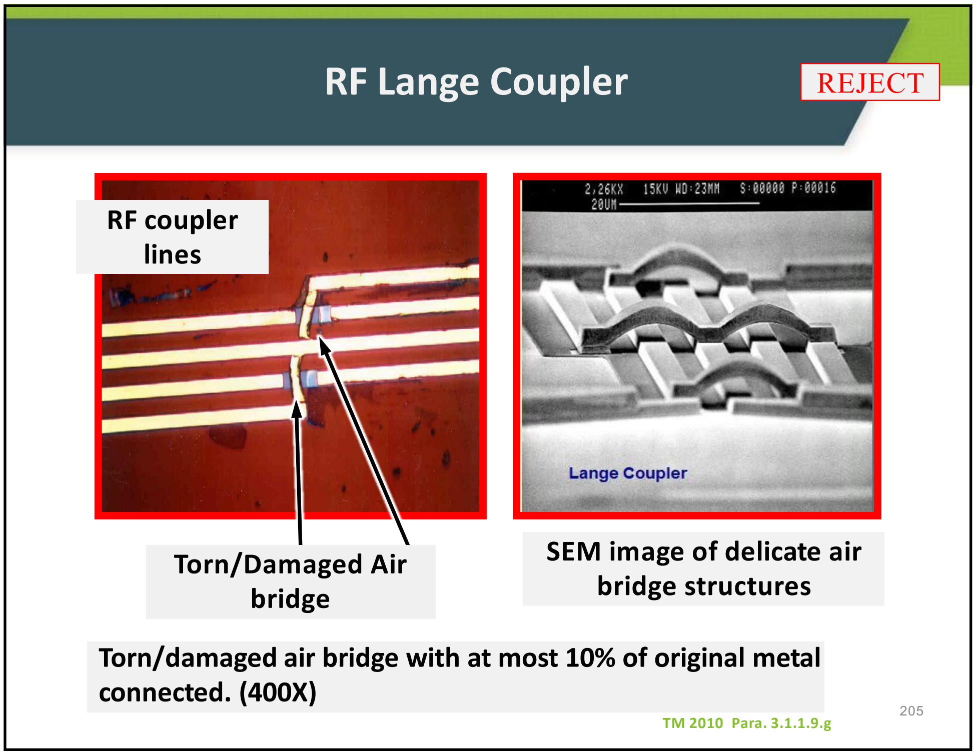
Post (Pin)
Diode

Depressed Air
Bridge

Short after
turn on due
to collapsed
Air Bridge

Air bridge appears to be depressed/damaged potential for metal shorting through underside passivation layer. (400X)

TM 2010 Para. 3.1.1.9.e



RF Lange Coupler

REJECT

RF coupler lines

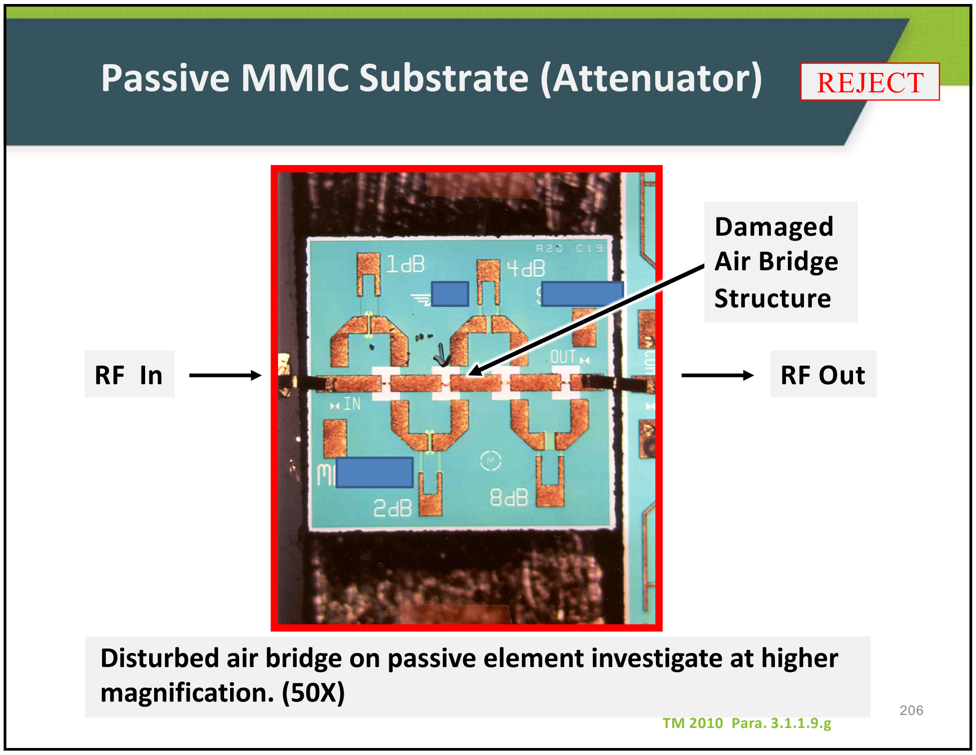
Torn/Damaged Air bridge

SEM image of delicate air bridge structures

Torn/damaged air bridge with at most 10% of original metal connected. (400X)

TM 2010 Para. 3.1.1.9.g

205



Passive MMIC Substrate (Attenuator)

REJECT

Damaged Air Bridge Structure

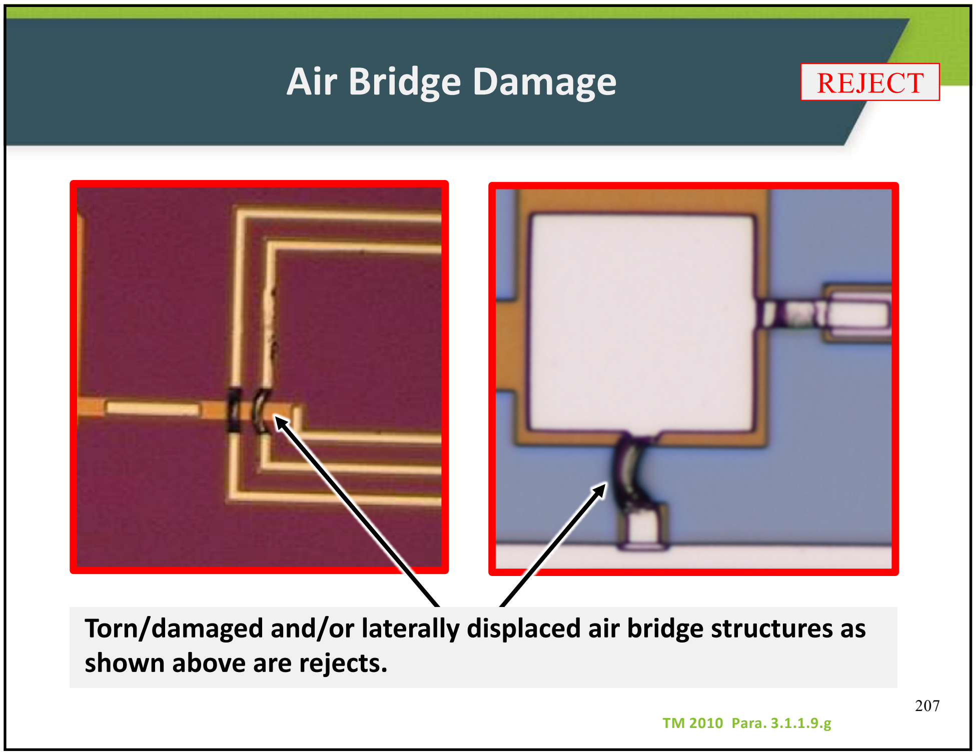
RF In

RF Out

Disturbed air bridge on passive element investigate at higher magnification. (50X)

TM 2010 Para. 3.1.1.9.g

206

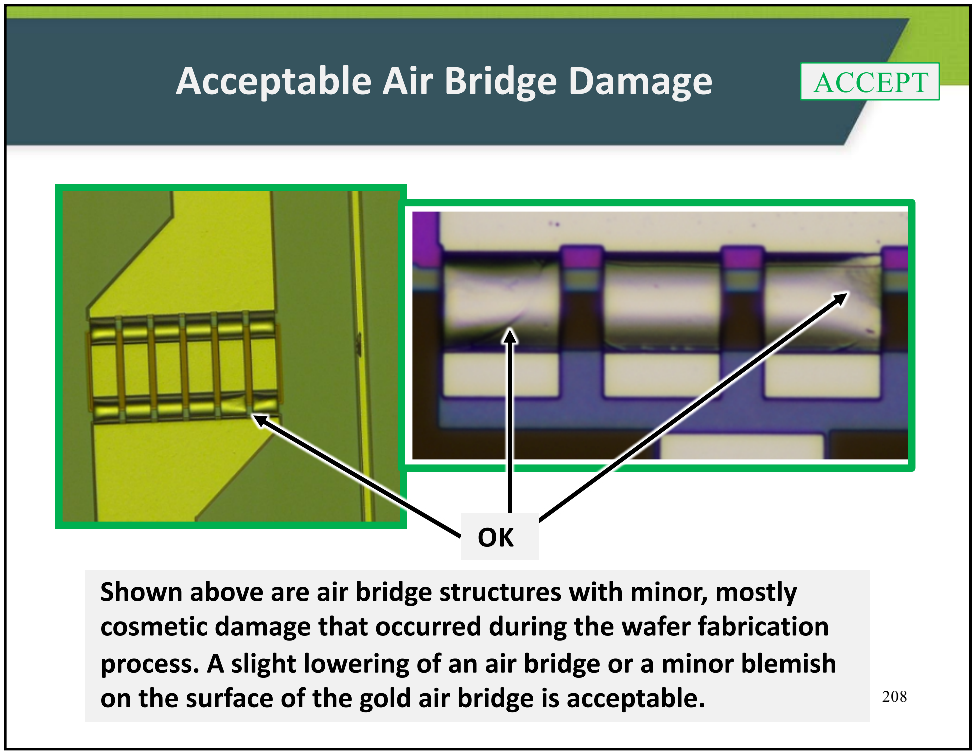


Air Bridge Damage

REJECT

Torn/damaged and/or laterally displaced air bridge structures as shown above are rejects.

TM 2010 Para. 3.1.1.9.g

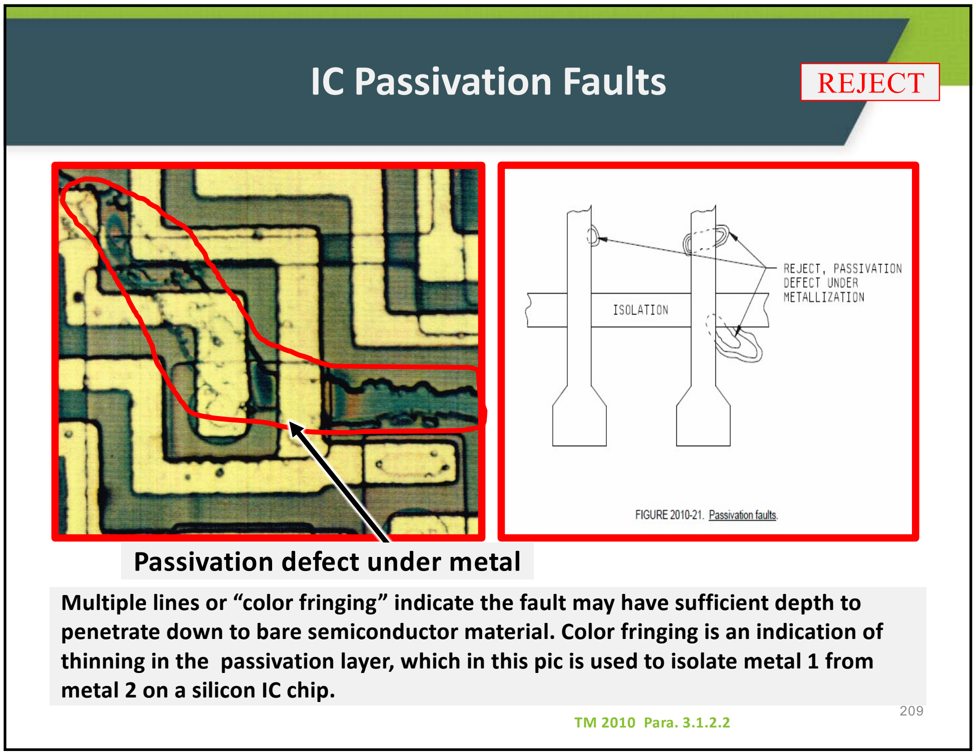


Acceptable Air Bridge Damage

ACCEPT

Shown above are air bridge structures with minor, mostly cosmetic damage that occurred during the wafer fabrication process. A slight lowering of an air bridge or a minor blemish on the surface of the gold air bridge is acceptable.

Course Notes



IC Passivation Faults

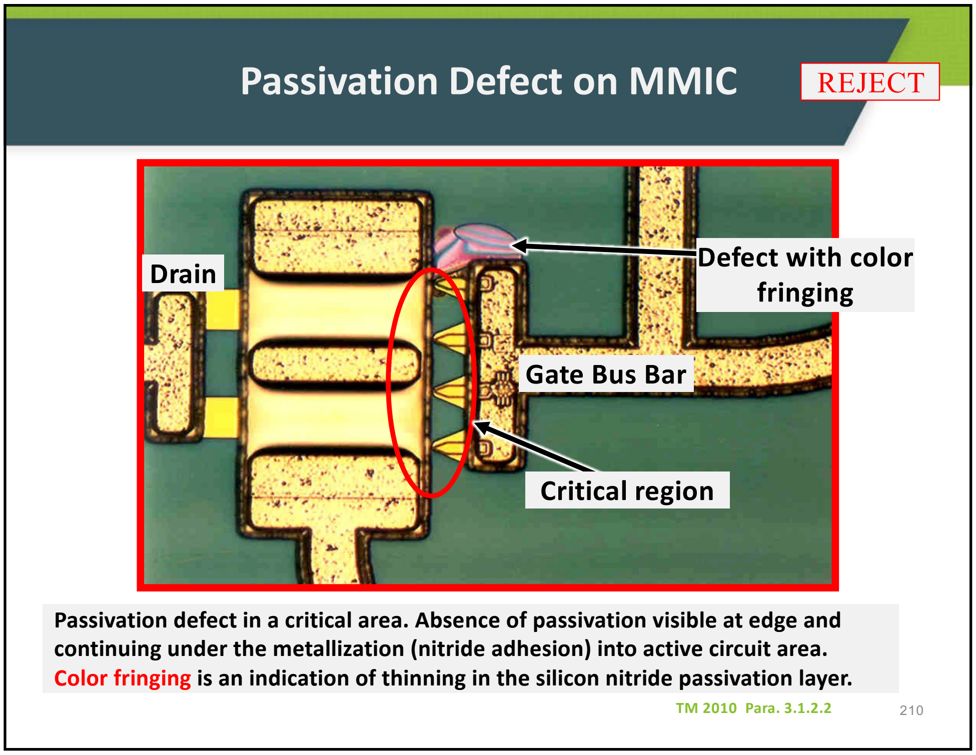
REJECT

FIGURE 2010-21. Passivation faults.

Passivation defect under metal

Multiple lines or “color fringing” indicate the fault may have sufficient depth to penetrate down to bare semiconductor material. Color fringing is an indication of thinning in the passivation layer, which in this pic is used to isolate metal 1 from metal 2 on a silicon IC chip.

TM 2010 Para. 3.1.2.2



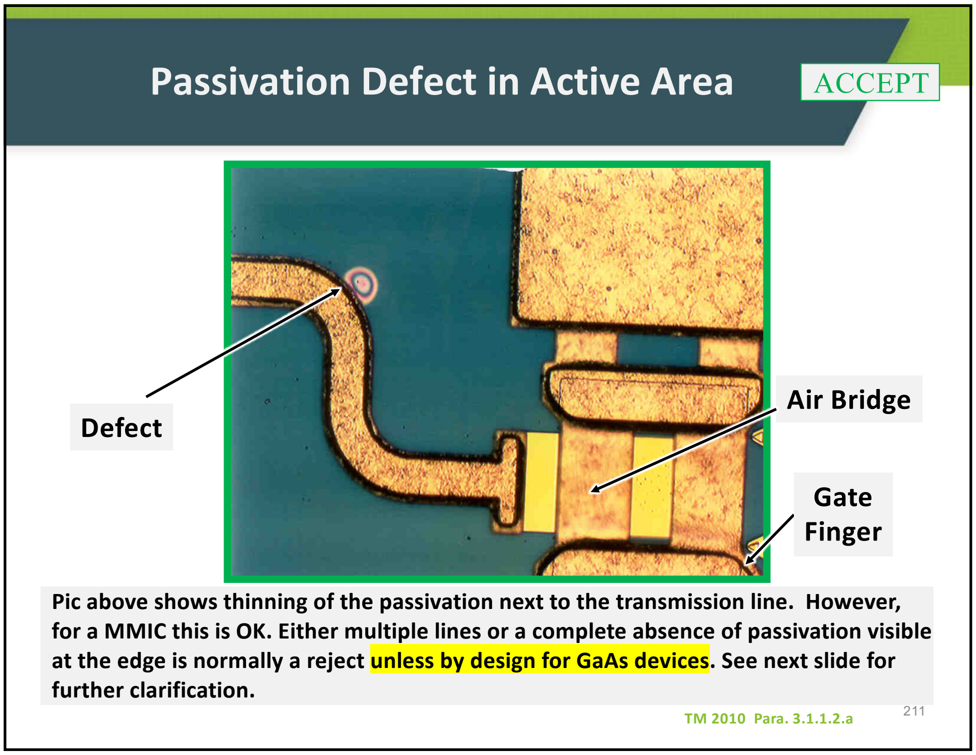
Passivation Defect on MMIC

REJECT

Passivation defect in a critical area. Absence of passivation visible at edge and continuing under the metallization (nitride adhesion) into active circuit area. Color fringing is an indication of thinning in the silicon nitride passivation layer.

TM 2010 Para. 3.1.2.2

Course Notes

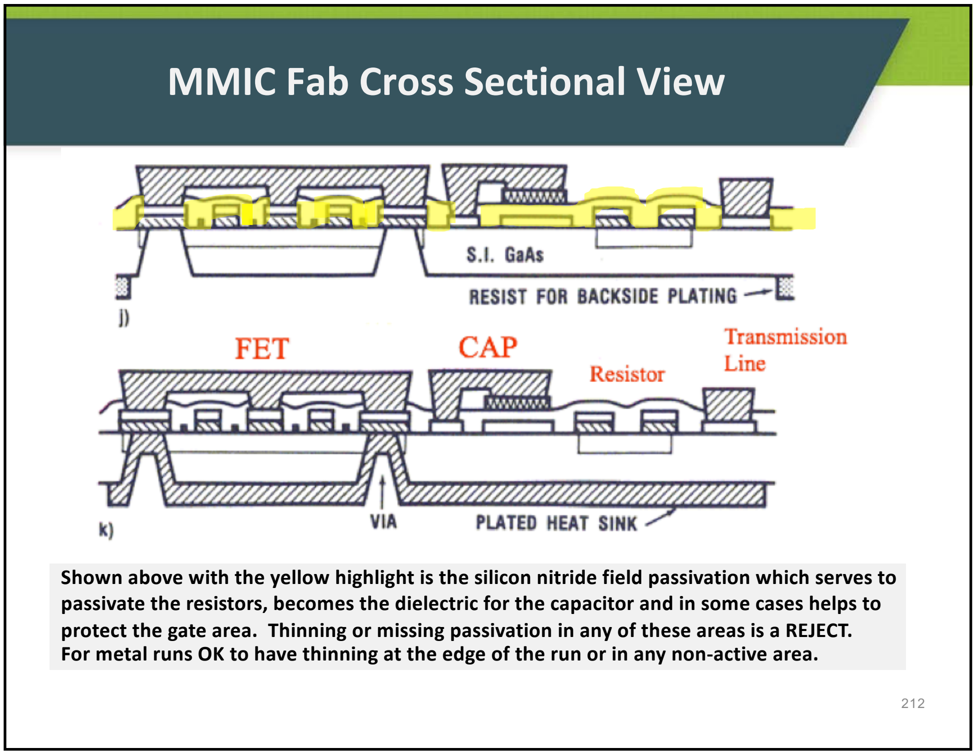


Passivation Defect in Active Area

ACCEPT

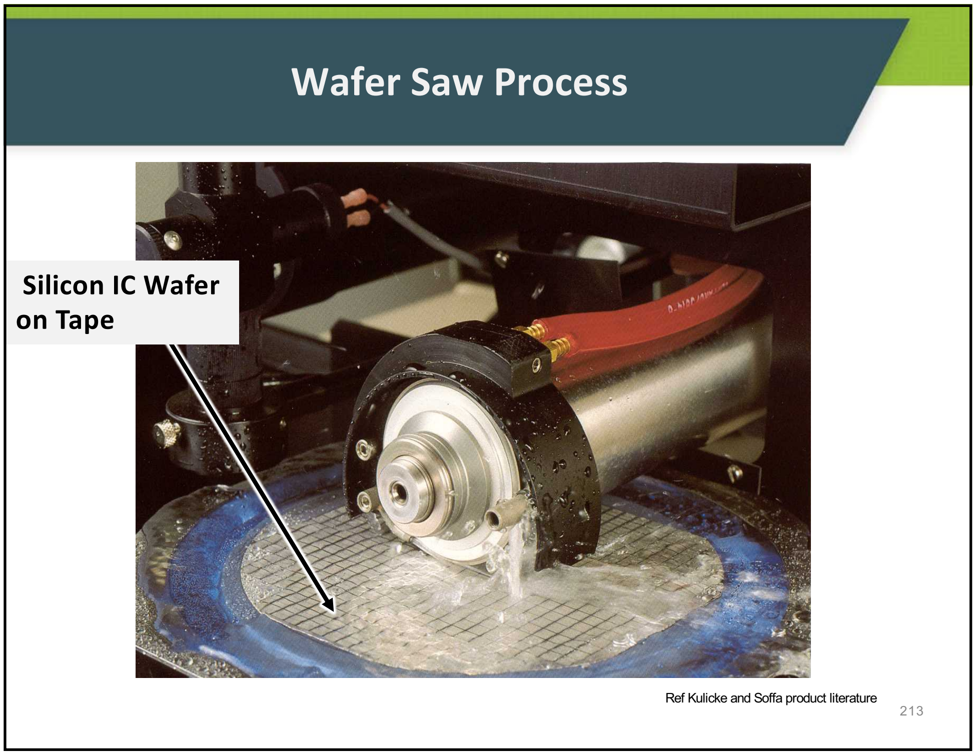
Pic above shows thinning of the passivation next to the transmission line. However, for a MMIC this is OK. Either multiple lines or a complete absence of passivation visible at the edge is normally a reject unless by design for GaAs devices. See next slide for further clarification.

TM 2010 Para. 3.1.1.2.a



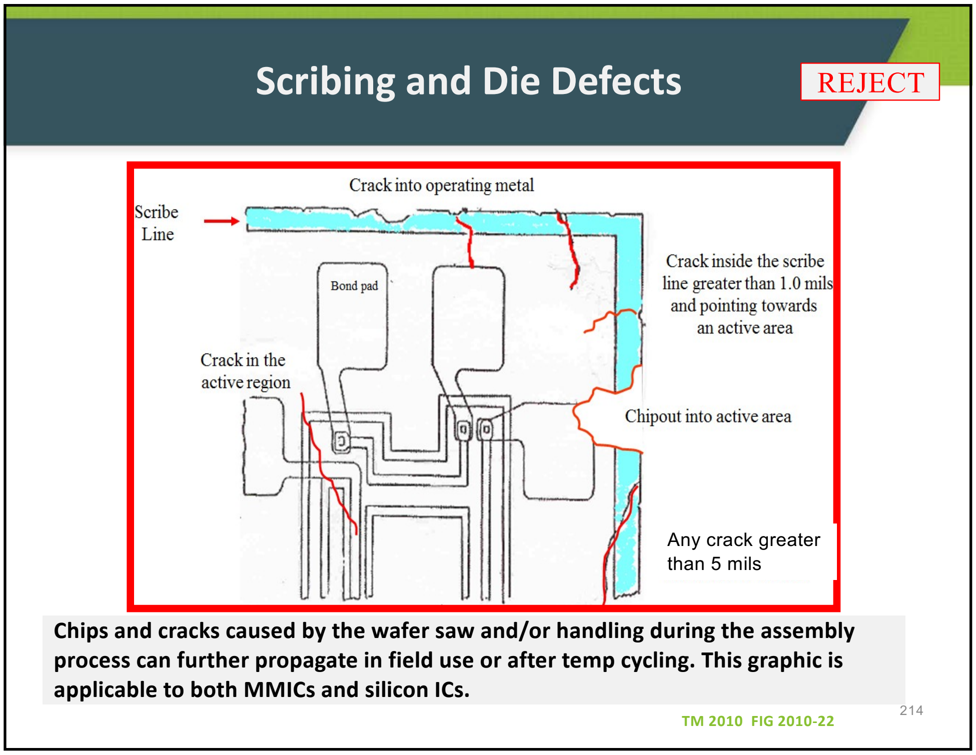
MMIC Fab Cross Sectional View

Shown above with the yellow highlight is the silicon nitride field passivation which serves to passivate the resistors, becomes the dielectric for the capacitor and in some cases helps to protect the gate area. Thinning or missing passivation in any of these areas is a REJECT. For metal runs OK to have thinning at the edge of the run or in any non-active area.



Wafer Saw Process

Ref Kulicke and Soffa product literature

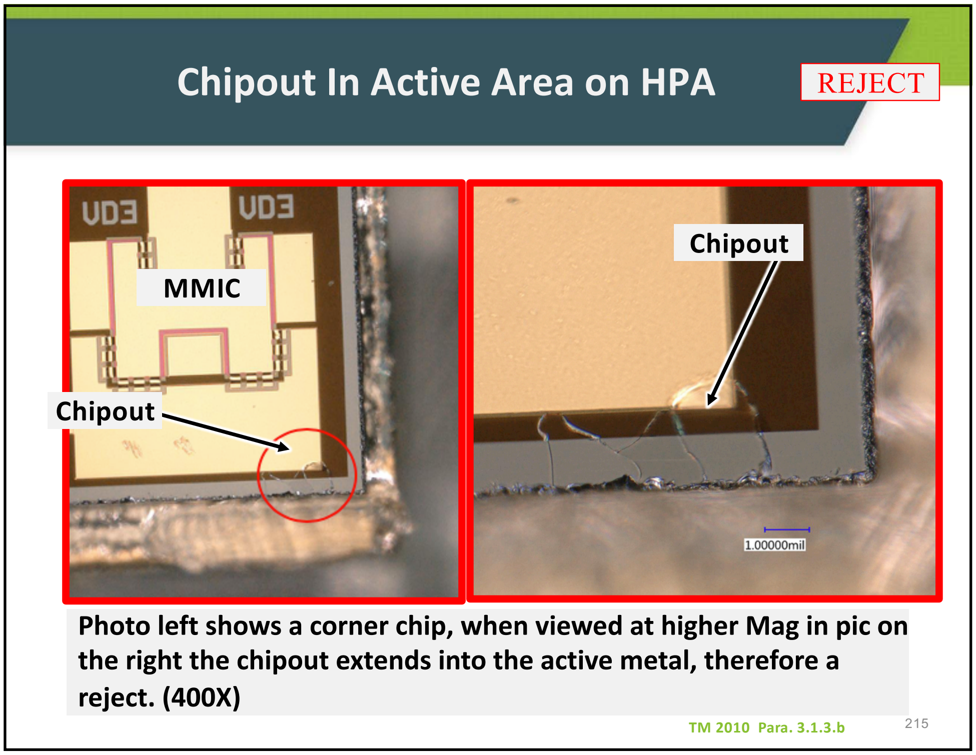


Scribing and Die Defects

REJECT

Chips and cracks caused by the wafer saw and/or handling during the assembly process can further propagate in field use or after temp cycling. This graphic is applicable to both MMICs and silicon ICs.

TM 2010 FIG 2010-22

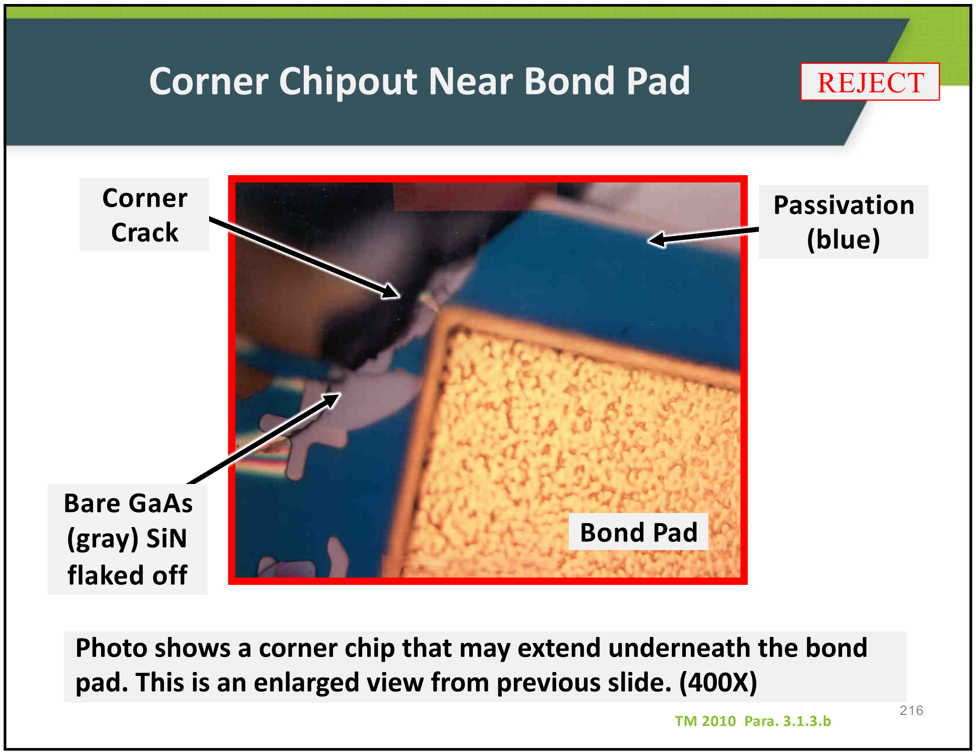


Chipout In Active Area on HPA

REJECT

Photo left shows a corner chip, when viewed at higher Mag in pic on the right the chipout extends into the active metal, therefore a reject. (400X)

TM 2010 Para. 3.1.3.b



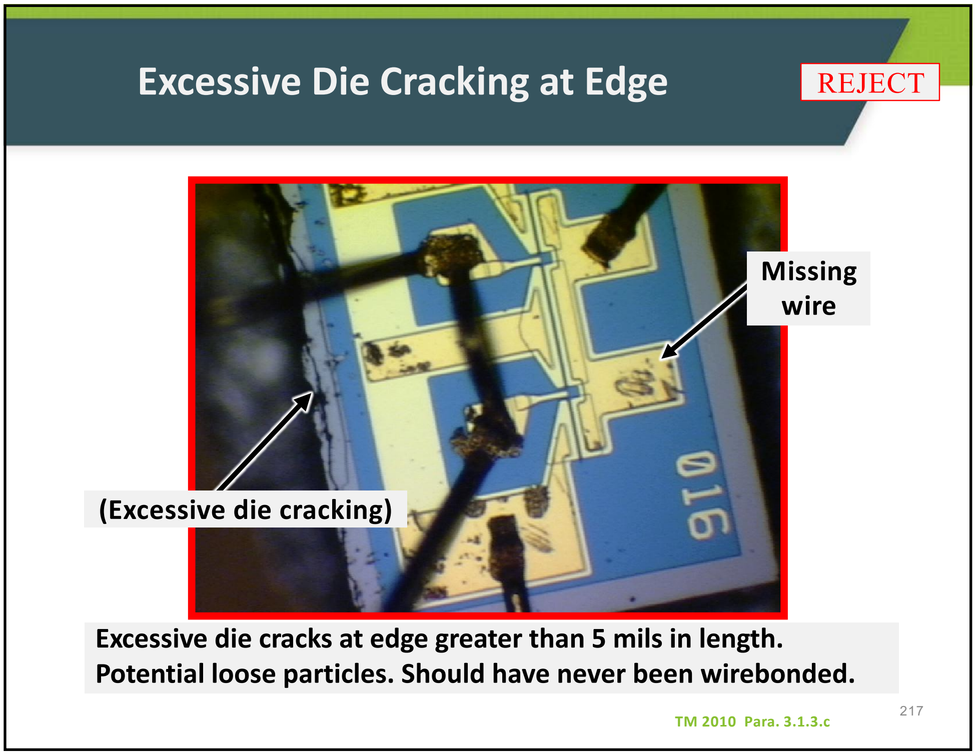
Corner Chipout Near Bond Pad

REJECT

Photo shows a corner chip that may extend underneath the bond pad. This is an enlarged view from previous slide. (400X)

TM 2010 Para. 3.1.3.b

Course Notes



Excessive Die Cracking at Edge

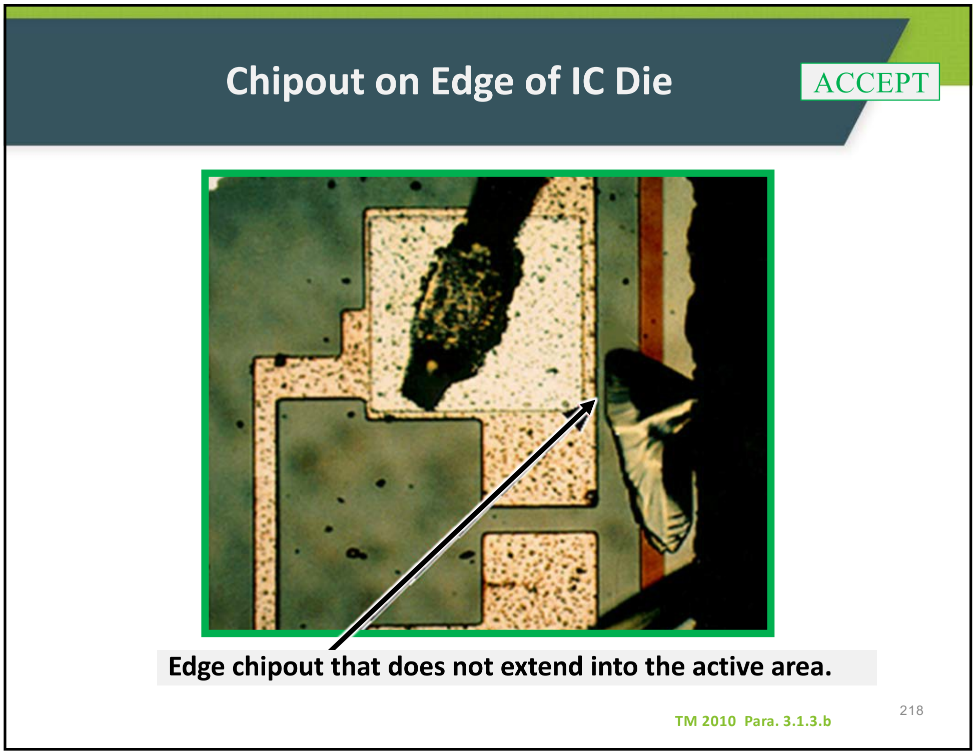
REJECT

Missing wire

(Excessive die cracking)

Excessive die cracks at edge greater than 5 mils in length. Potential loose particles. Should have never been wirebonded.

TM 2010 Para. 3.1.3.c



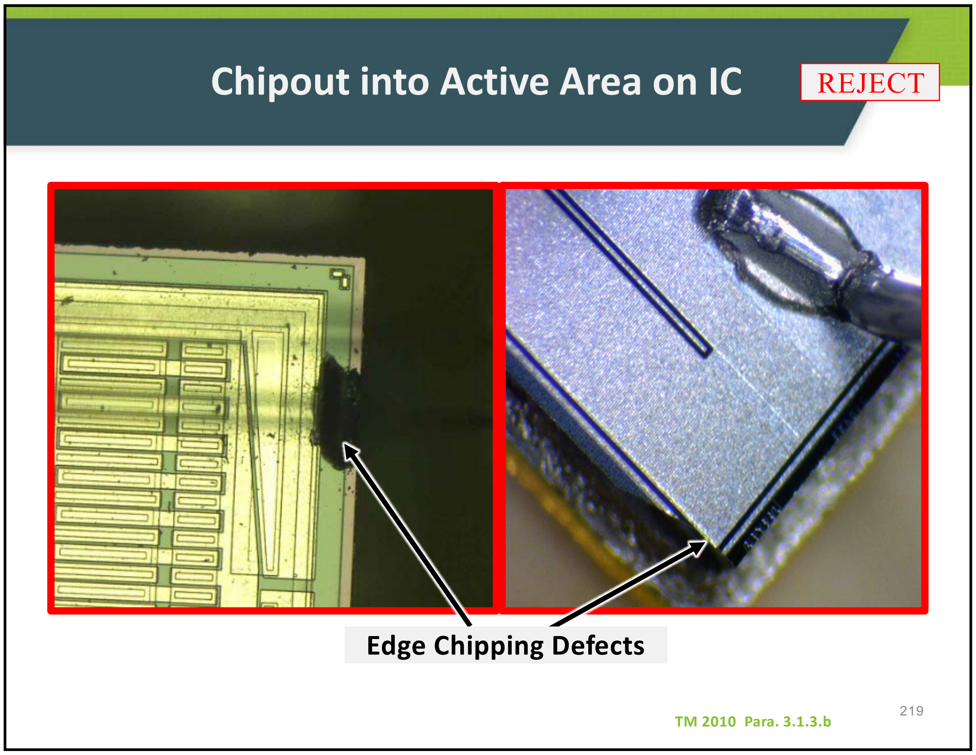
Chipout on Edge of IC Die

ACCEPT

Edge chipout that does not extend into the active area.

TM 2010 Para. 3.1.3.b

Course Notes

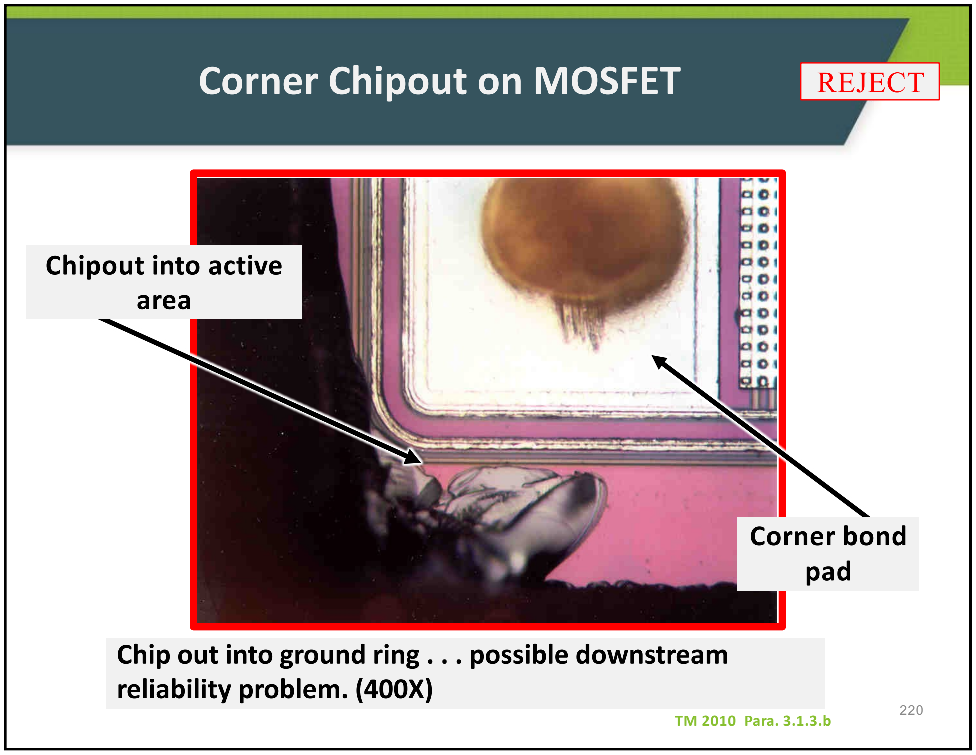


Chipout into Active Area on IC

REJECT

Edge Chipping Defects

TM 2010 Para. 3.1.3.b



Corner Chipout on MOSFET

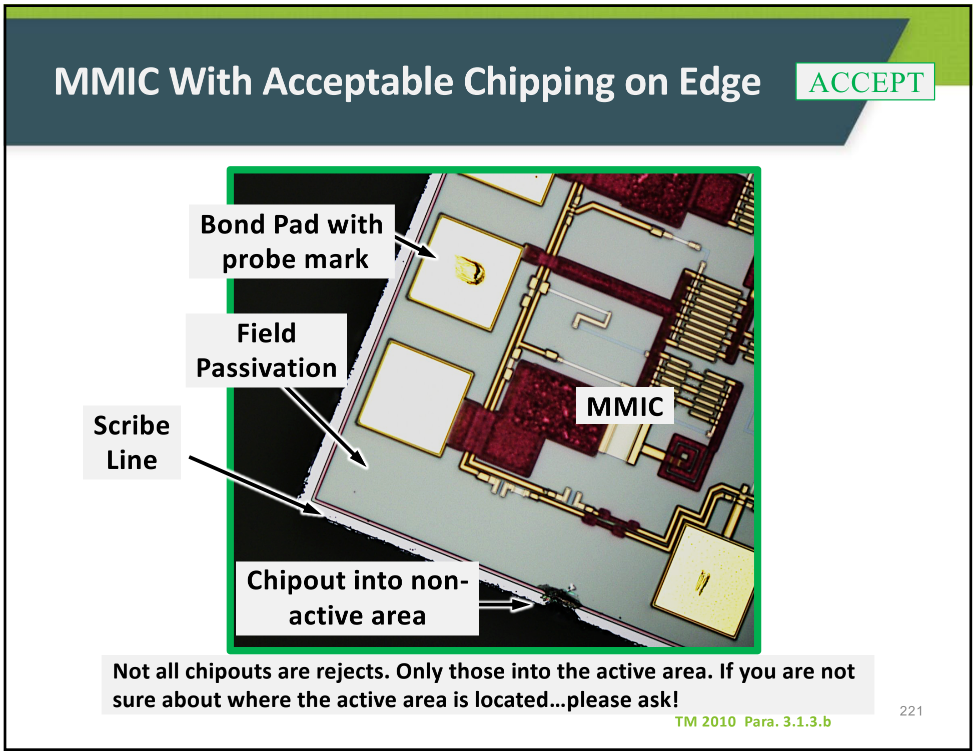
REJECT

Chipout into active area

Corner bond pad

Chip out into ground ring . . . possible downstream reliability problem. (400X)

TM 2010 Para. 3.1.3.b

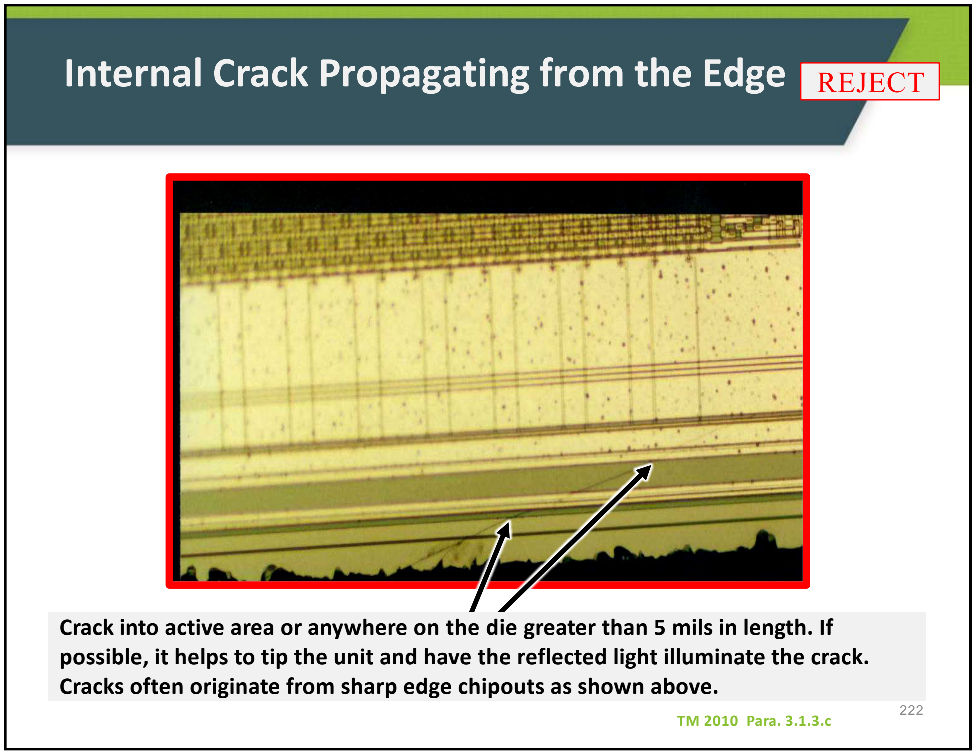


MMIC With Acceptable Chipping on Edge

ACCEPT

Not all chipouts are rejects. Only those into the active area. If you are not sure about where the active area is located…please ask!

TM 2010 Para. 3.1.3.b

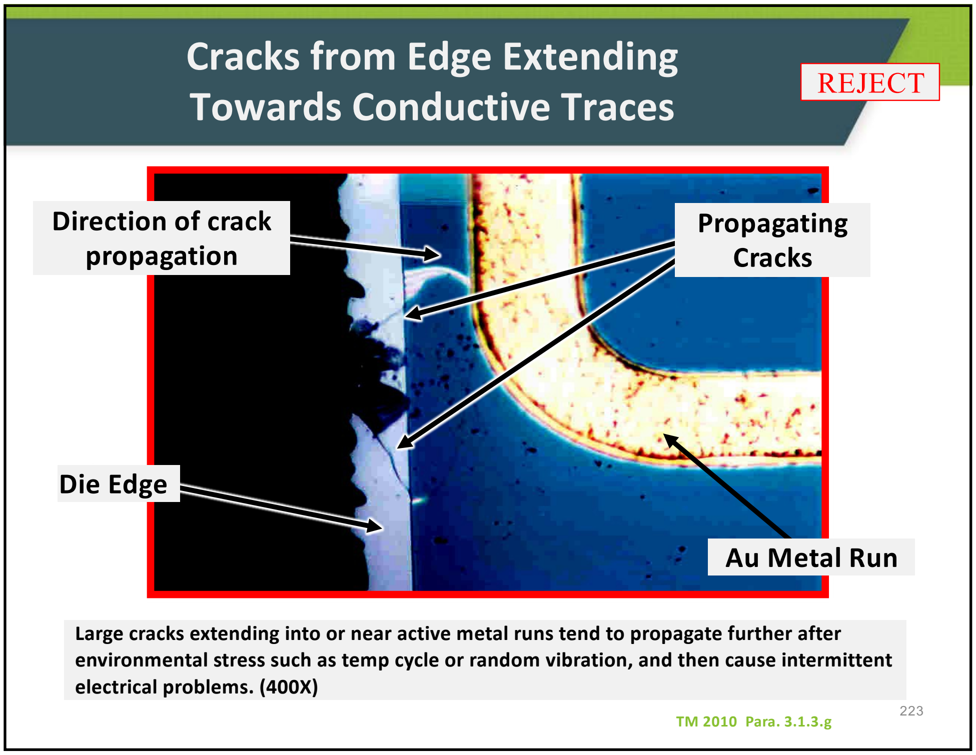


Internal Crack Propagating from the Edge

REJECT

Crack into active area or anywhere on the die greater than 5 mils in length. If possible, it helps to tip the unit and have the reflected light illuminate the crack. Cracks often originate from sharp edge chipouts as shown above.

TM 2010 Para. 3.1.3.c



Cracks from Edge Extending Towards Conductive Traces

REJECT

Direction of crack propagation

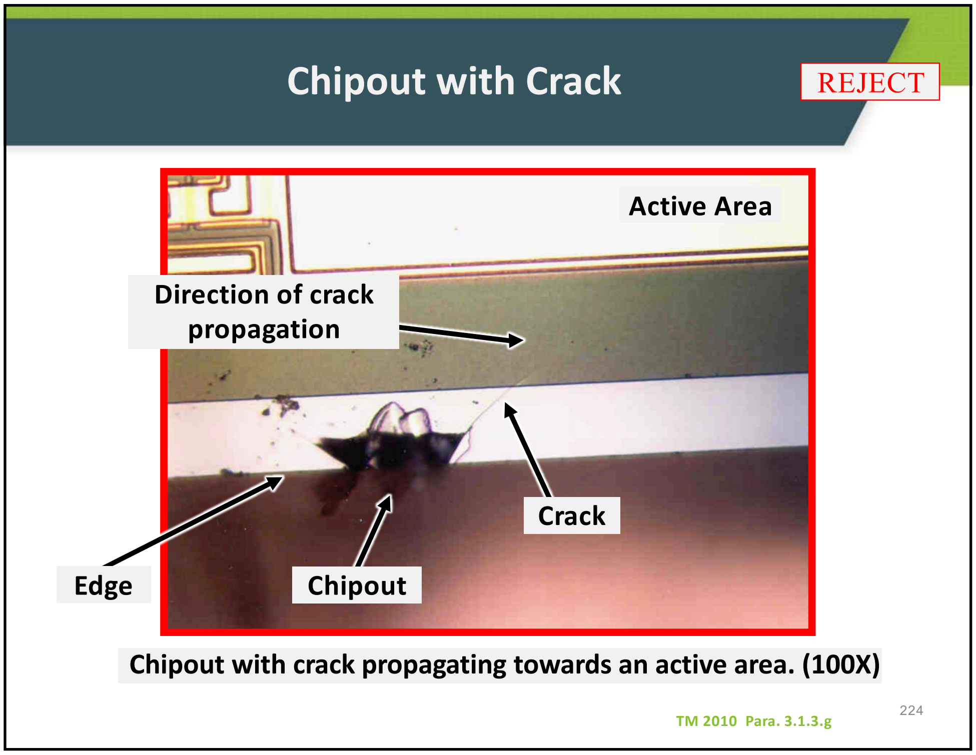
Propagating Cracks

Die Edge

Au Metal Run

Large cracks extending into or near active metal runs tend to propagate further after environmental stress such as temp cycle or random vibration, and then cause intermittent electrical problems. (400X)

TM 2010 Para. 3.1.3.g



Chipout with Crack

REJECT

Active Area

Direction of crack propagation

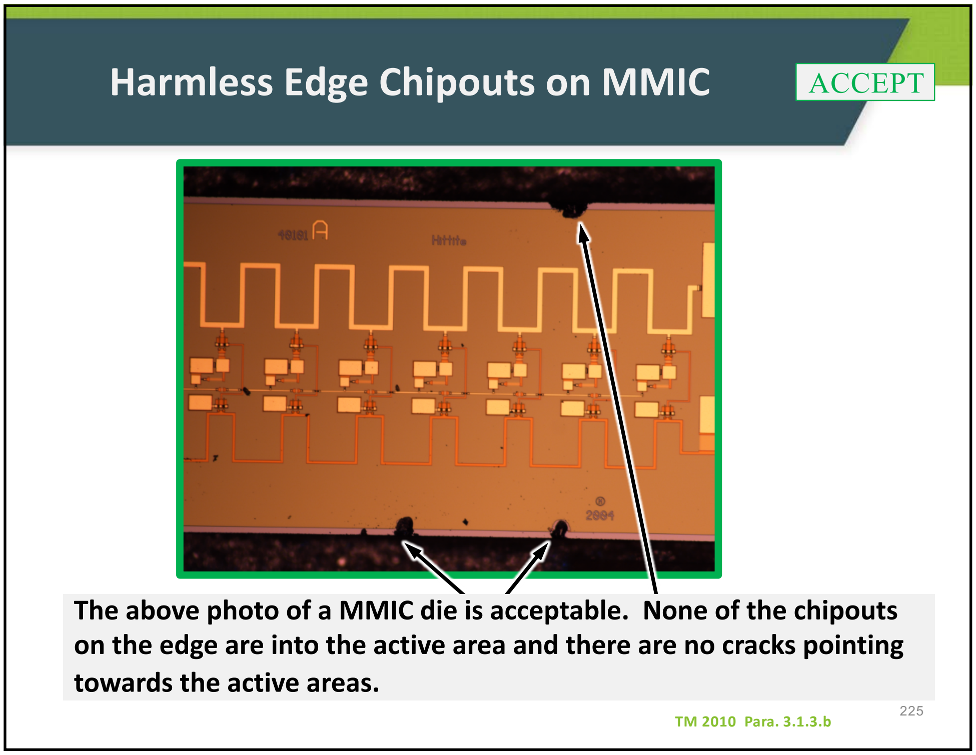
Crack

Edge

Chipout

Chipout with crack propagating towards an active area. (100X)

TM 2010 Para. 3.1.3.g

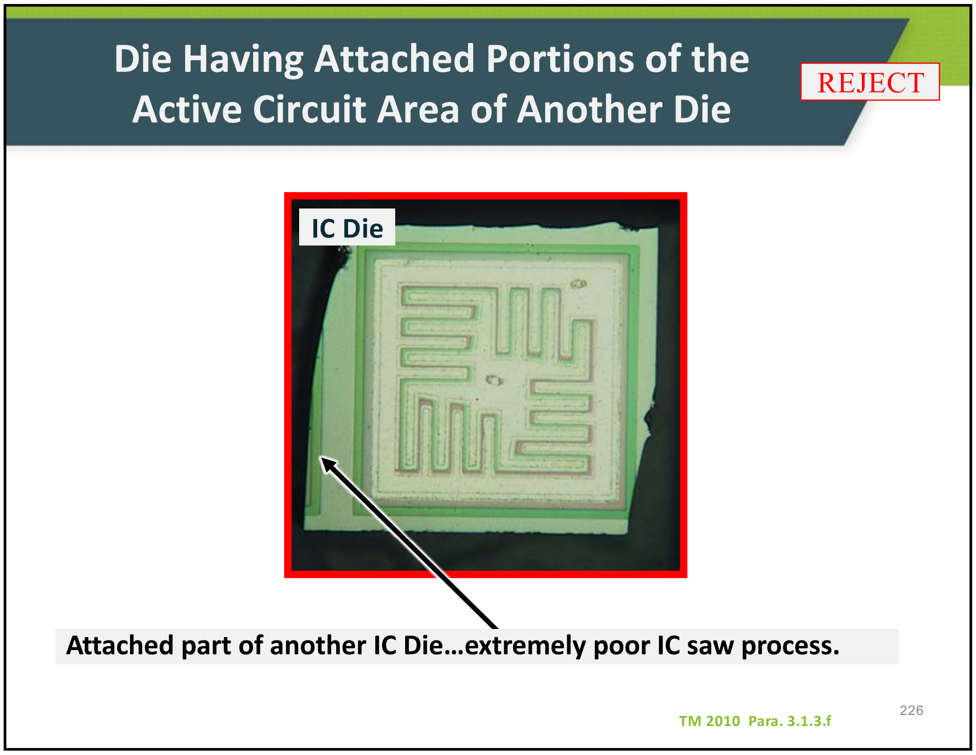


Harmless Edge Chipouts on MMIC

ACCEPT

The above photo of a MMIC die is acceptable. None of the chipouts on the edge are into the active area and there are no cracks pointing towards the active areas.

TM 2010 Para. 3.1.3.b



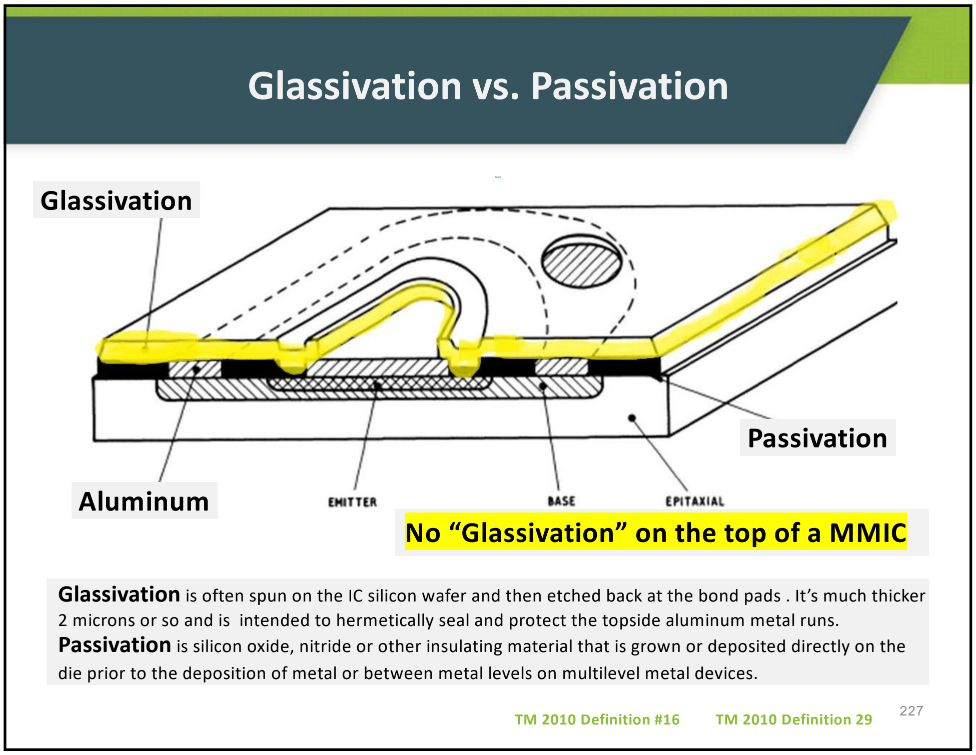
Die Having Attached Portions of the Active Circuit Area of Another Die

REJECT

Attached part of another IC Die…extremely poor IC saw process.

TM 2010 Para. 3.1.3.f

Course Notes



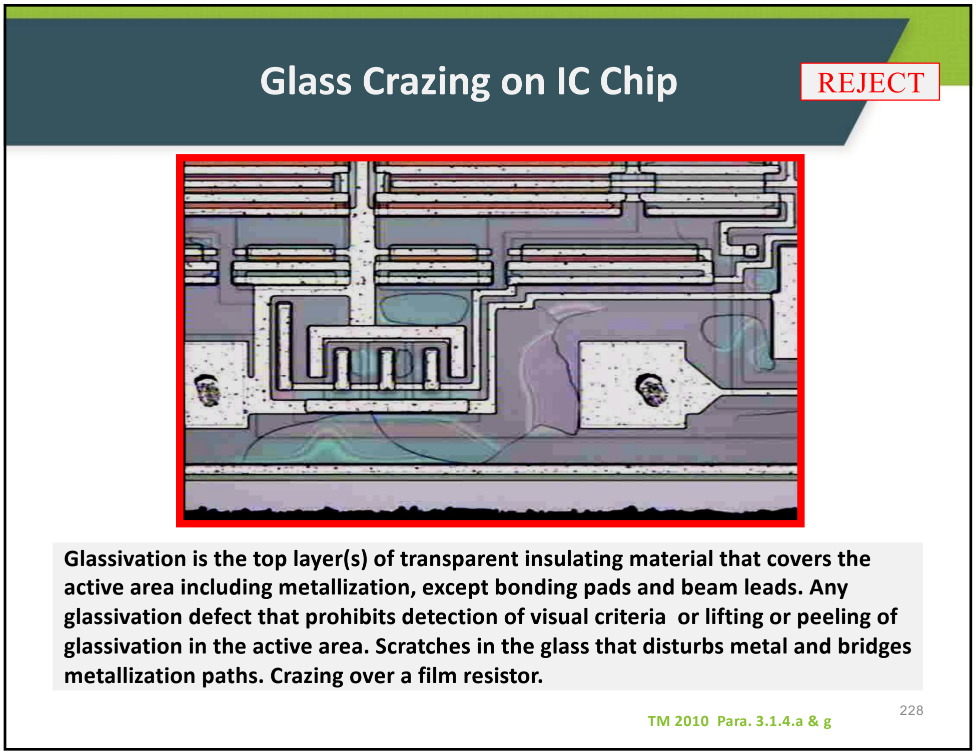
Glassivation vs. Passivation

No "Glassivation" on the top of a MMIC

Glassivation is often spun on the IC silicon wafer and then etched back at the bond pads . It's much thicker 2 microns or so and is intended to hermetically seal and protect the topside aluminum metal runs.

Passivation is silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal or between metal levels on multilevel metal devices.

TM 2010 Definition #16 TM 2010 Definition 29

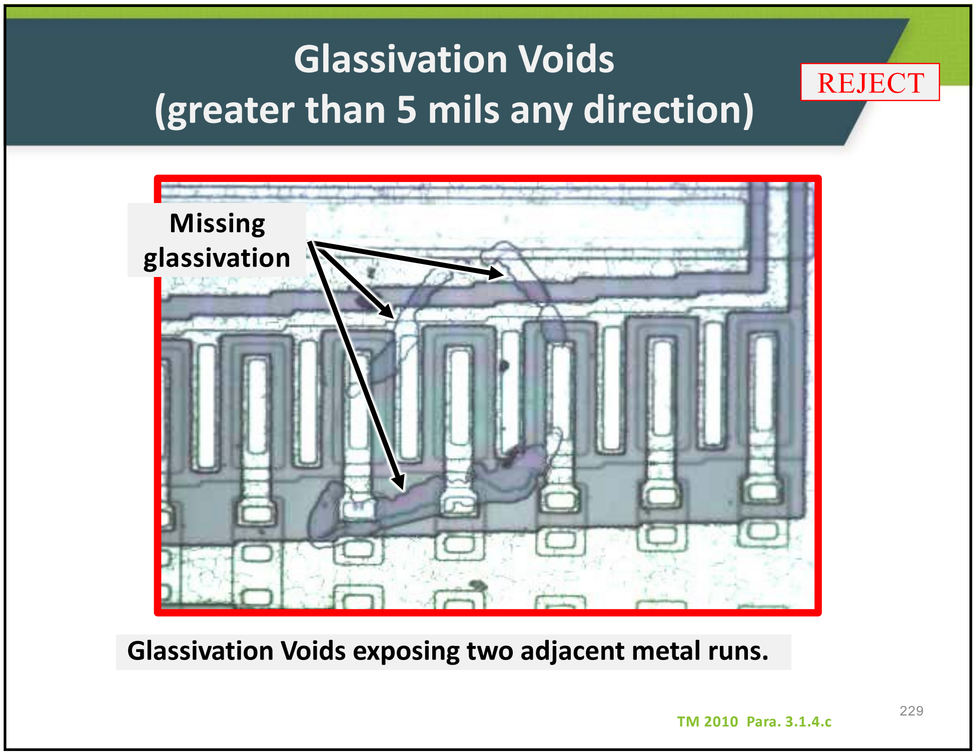


Glass Crazing on IC Chip

REJECT

Glassivation is the top layer(s) of transparent insulating material that covers the active area including metallization, except bonding pads and beam leads. Any glassivation defect that prohibits detection of visual criteria or lifting or peeling of glassivation in the active area. Scratches in the glass that disturbs metal and bridges metallization paths. Crazing over a film resistor.

TM 2010 Para. 3.1.4.a & g



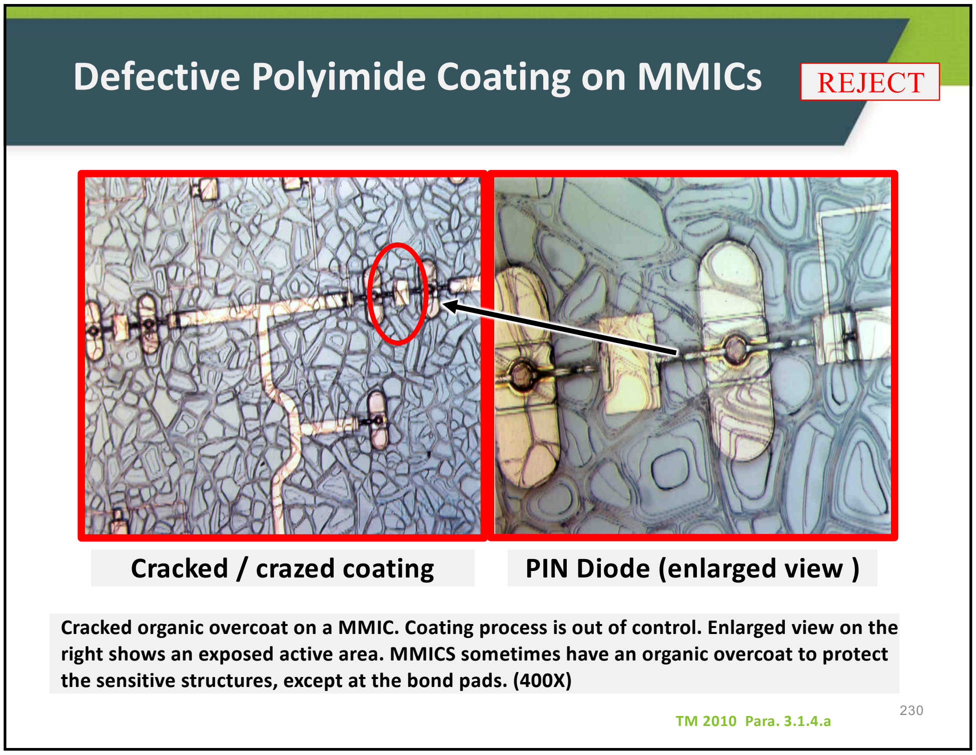
Glassivation Voids (greater than 5 mils any direction)

REJECT

Missing glassivation

Glassivation Voids exposing two adjacent metal runs.

TM 2010 Para. 3.1.4.c



Defective Polyimide Coating on MMICs

REJECT

Cracked / crazed coating

PIN Diode (enlarged view)

Cracked organic overcoat on a MMIC. Coating process is out of control. Enlarged view on the right shows an exposed active area. MMICS sometimes have an organic overcoat to protect the sensitive structures, except at the bond pads. (400X)

TM 2010 Para. 3.1.4.a

TM 2032 Passive Elements

Per TM 2017 passive elements (including substrates) shall be examined in accordance with MIL-STD-883, method 2032.

Section 3.1	Thin Film Resistors (100 to 200X)
Section 3.2	Thick Film Resistors (10 to 60X)
Section 3.3	Capacitor Inspection Non-Planar MLCC (Multi Layer Chip Capacitors) Both low and high Mag
Section 3.4	Inductor and Transformer Inspection
Section 3.5	Surface Acoustic Wave (SAW) element inspection

Thin Film vs. Thick Film

Different processes used to create passive circuit elements such as resistors, capacitors and inductors.

Thick film is thicker, but also appears bumpy under a microscope and slightly ragged along the edge.

Thin films are surface smooth and the lines are edge sharp…. better for high frequency microwave applications.

CAUTION: TM 2032 inspection criteria is organized according to technology . . . make sure you know what you are looking at! If you don't know, ask

Thick film - is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.

Thin film - is conductive, resistive or dielectric material, usually less than 50,000Å in thickness that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.

Thin Film Process

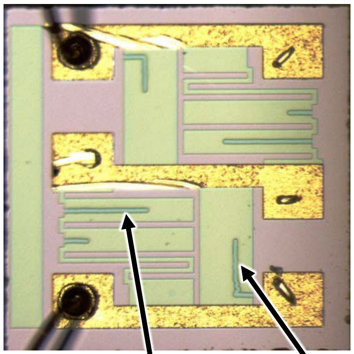
MRC Sputtering System

Plating bath

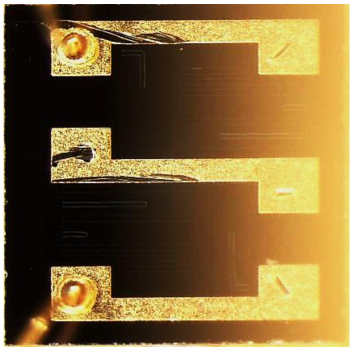
Substrates are sputtered or vapor deposited with a thin film seed layer of metal then electroplated with Ni/Au in a heated bath of plating solution. Typical mil spec plating is 50 microinches of soft gold over 200 microinches of nickel. Tantalum nitride and NiCr are typical resistor materials used in the industry.

Thin Film Resistor Trims

Light Field

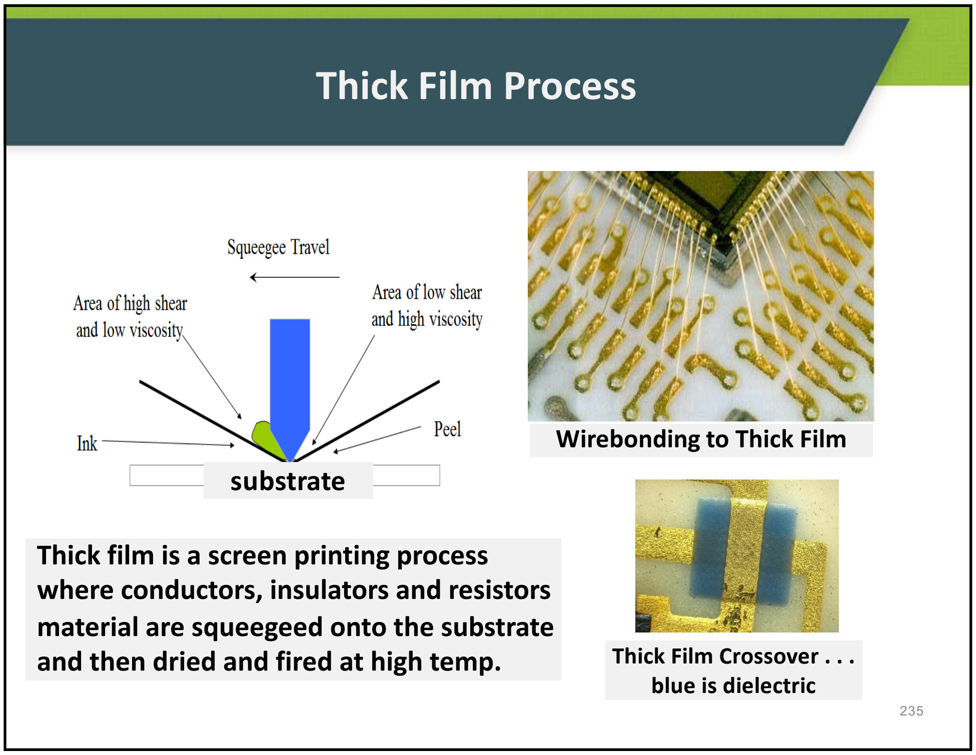


Dark Field



Top Hat Trim

Clean resistor trim into tantalum nitride . . . clean kerf

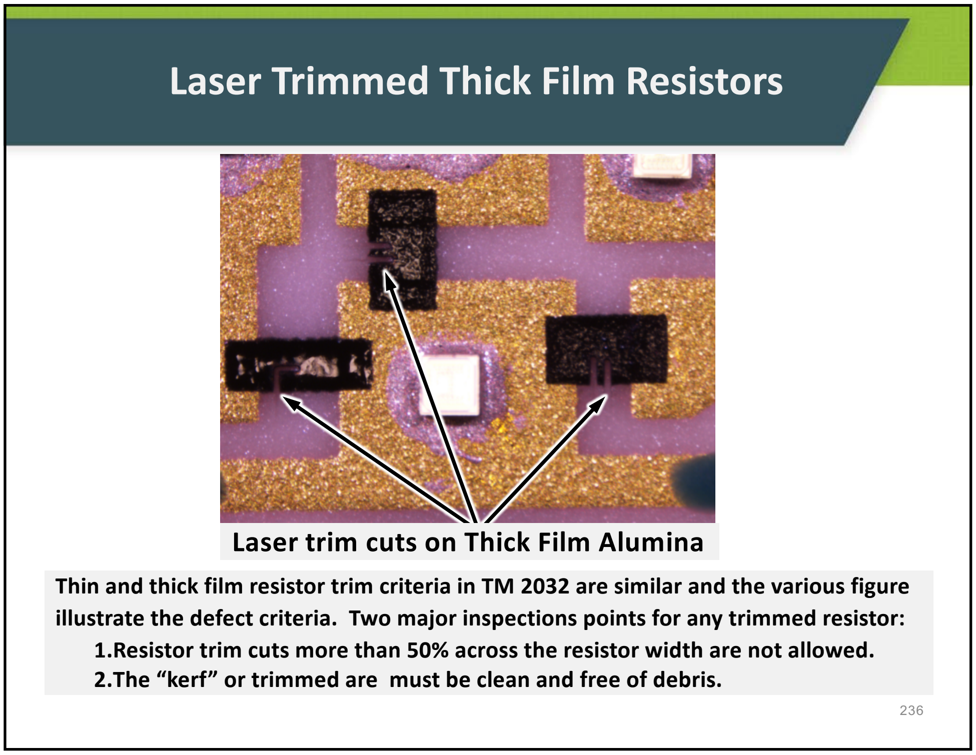


Thick Film Process

Thick film is a screen printing process where conductors, insulators and resistors material are squeegeed onto the substrate and then dried and fired at high temp.

Wirebonding to Thick Film

Thick Film Crossover . . . blue is dielectric



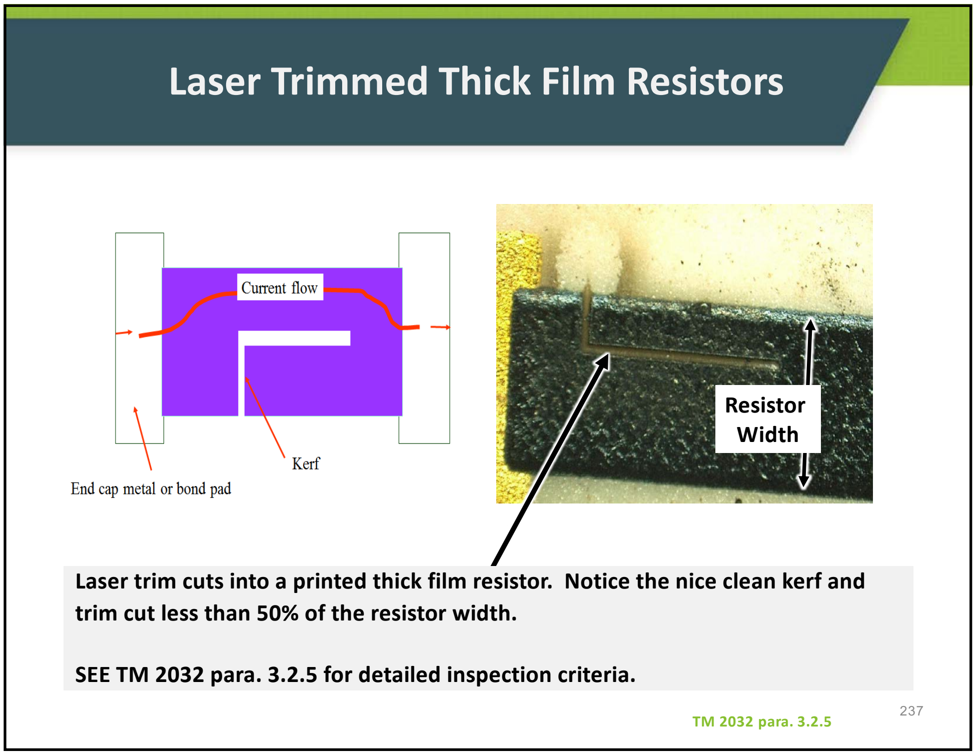
Laser Trimmed Thick Film Resistors

Laser trim cuts on Thick Film Alumina

Thin and thick film resistor trim criteria in TM 2032 are similar and the various figure illustrate the defect criteria. Two major inspections points for any trimmed resistor:

1. Resistor trim cuts more than 50% across the resistor width are not allowed.
2. The “kerf” or trimmed are must be clean and free of debris.

Course Notes

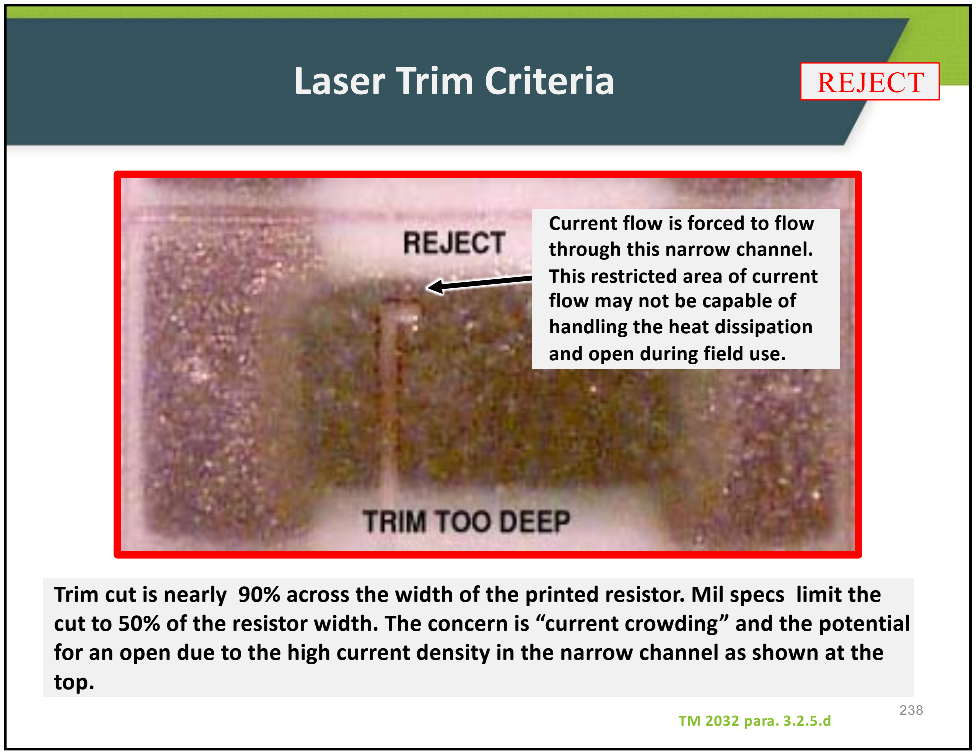


Laser Trimmed Thick Film Resistors

Laser trim cuts into a printed thick film resistor. Notice the nice clean kerf and trim cut less than 50% of the resistor width.

SEE TM 2032 para. 3.2.5 for detailed inspection criteria.

TM 2032 para. 3.2.5



Laser Trim Criteria

REJECT

Current flow is forced to flow through this narrow channel. This restricted area of current flow may not be capable of handling the heat dissipation and open during field use.

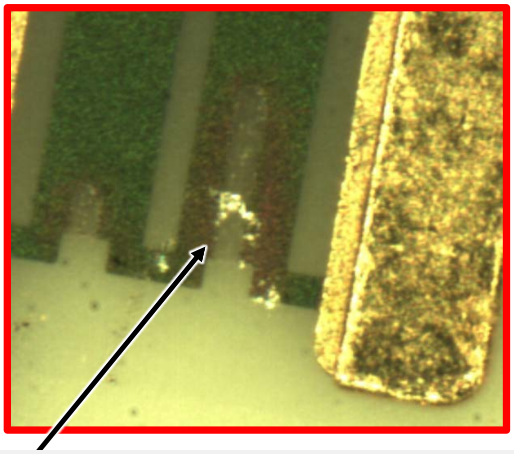
Trim cut is nearly 90% across the width of the printed resistor. Mil specs limit the cut to 50% of the resistor width. The concern is “current crowding” and the potential for an open due to the high current density in the narrow channel as shown at the top.

TM 2032 para. 3.2.5.d

Course Notes

Silver Epoxy in Trim Kerf

REJECT

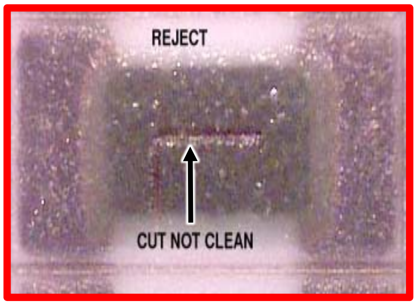


Silver epoxy bridging the laser trim kerf of a thick film resistor. This may have occurred during assembly or a rework process. This is considered foreign material or detritus and changes the resistor value.

TM 2032 para. 3.2.5.b

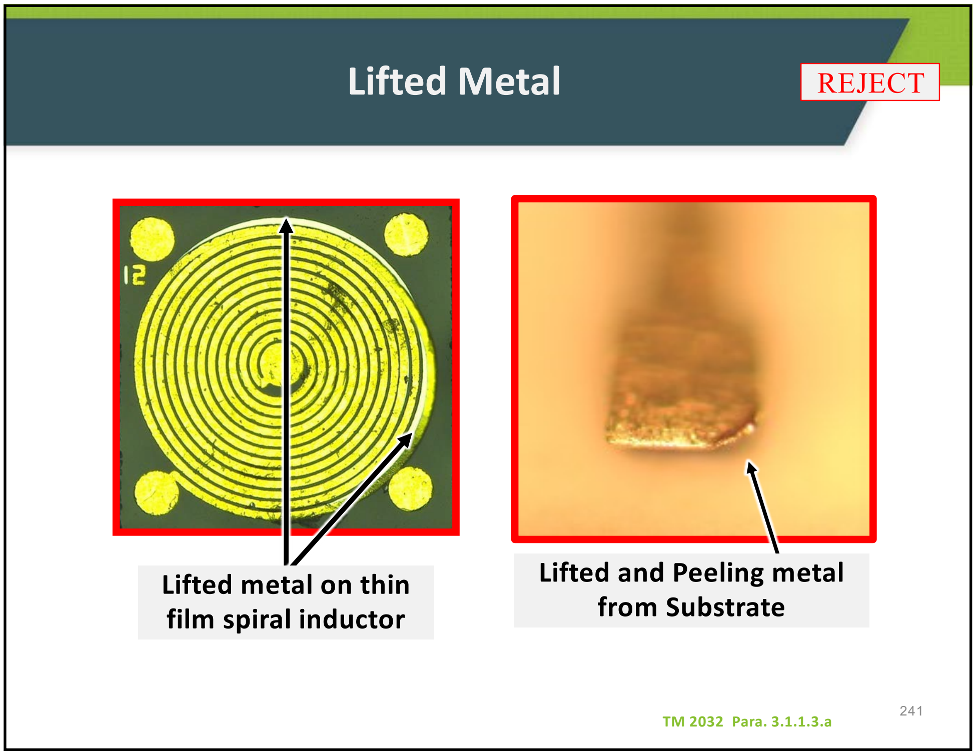
Laser Trim Criteria "Detritus in the Kerf"

REJECT



In both of the above photos there is evidence of material bridging across the kerf area. A good laser trim cut should produce a clean-cut path with no residual resistor material remaining in the cut area.

TM 2032 para. 3.2.5.b



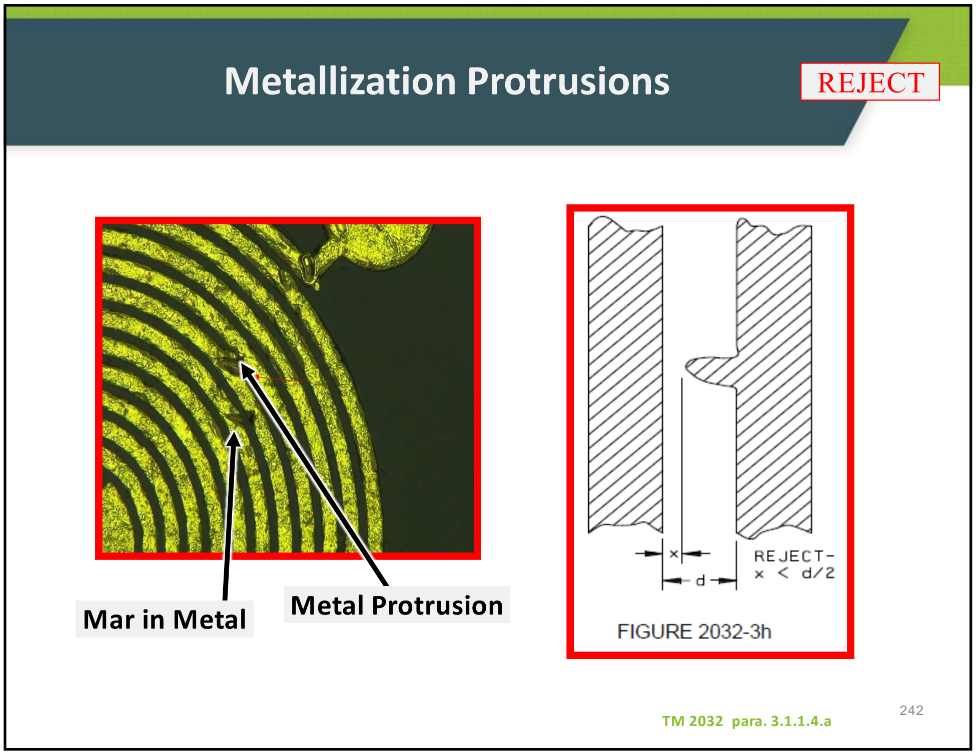
Lifted Metal

REJECT

Lifted metal on thin film spiral inductor

Lifted and Peeling metal from Substrate

TM 2032 Para. 3.1.1.3.a



Metallization Protrusions

REJECT

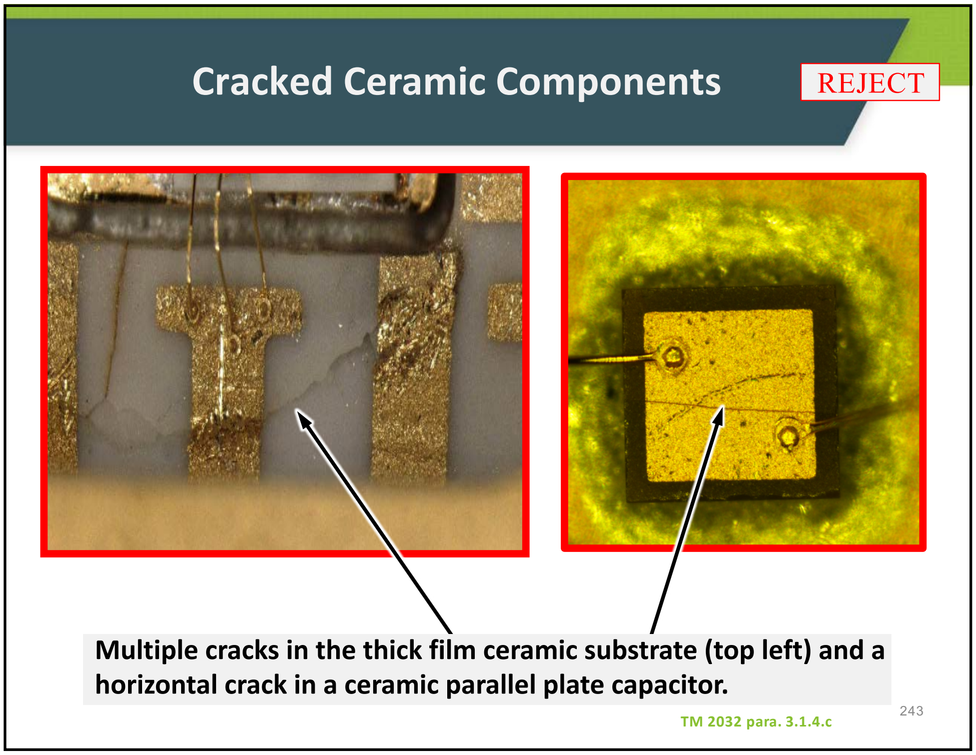
Mar in Metal

Metal Protrusion

FIGURE 2032-3h

TM 2032 para. 3.1.1.4.a

Course Notes

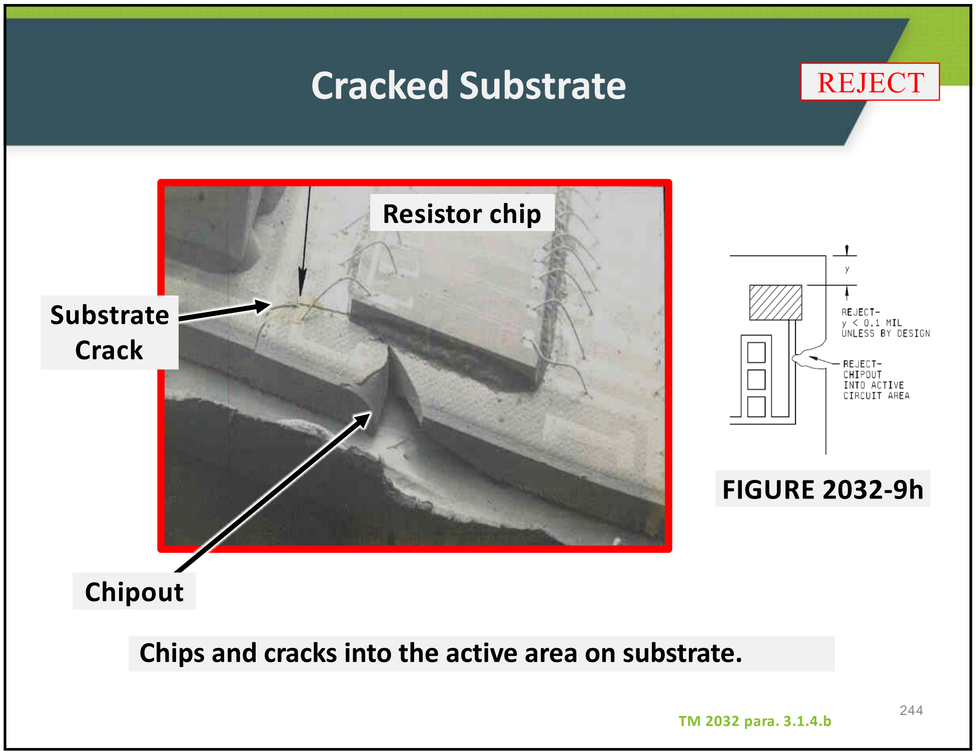


Cracked Ceramic Components

REJECT

Multiple cracks in the thick film ceramic substrate (top left) and a horizontal crack in a ceramic parallel plate capacitor.

TM 2032 para. 3.1.4.c



Cracked Substrate

REJECT

Resistor chip

Substrate Crack

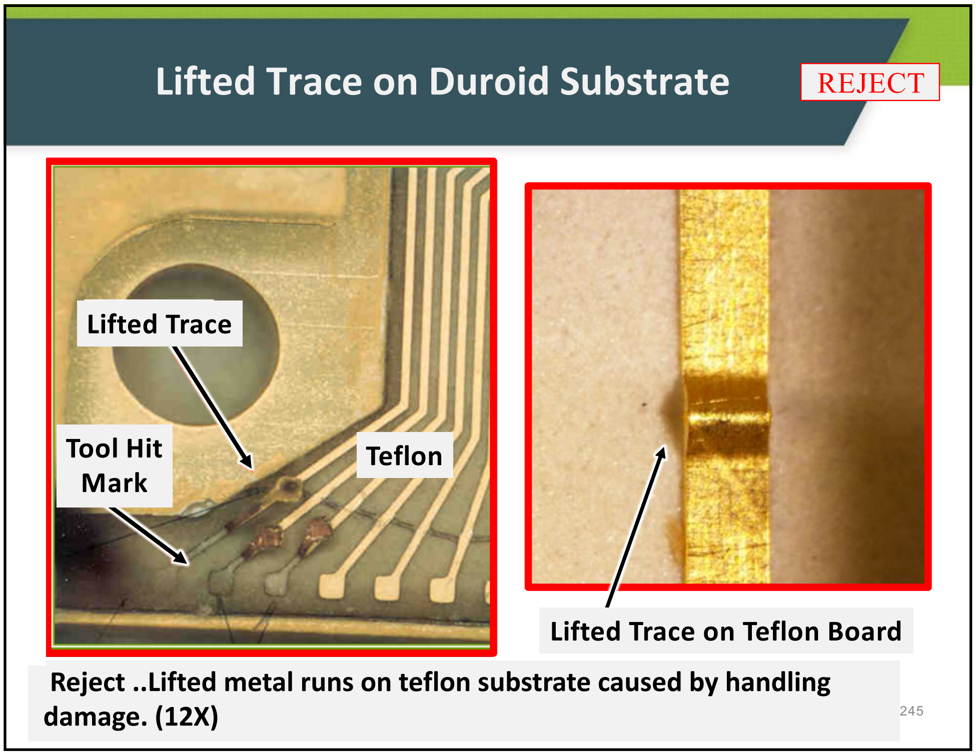
Chipout

FIGURE 2032-9h

Chips and cracks into the active area on substrate.

TM 2032 para. 3.1.4.b

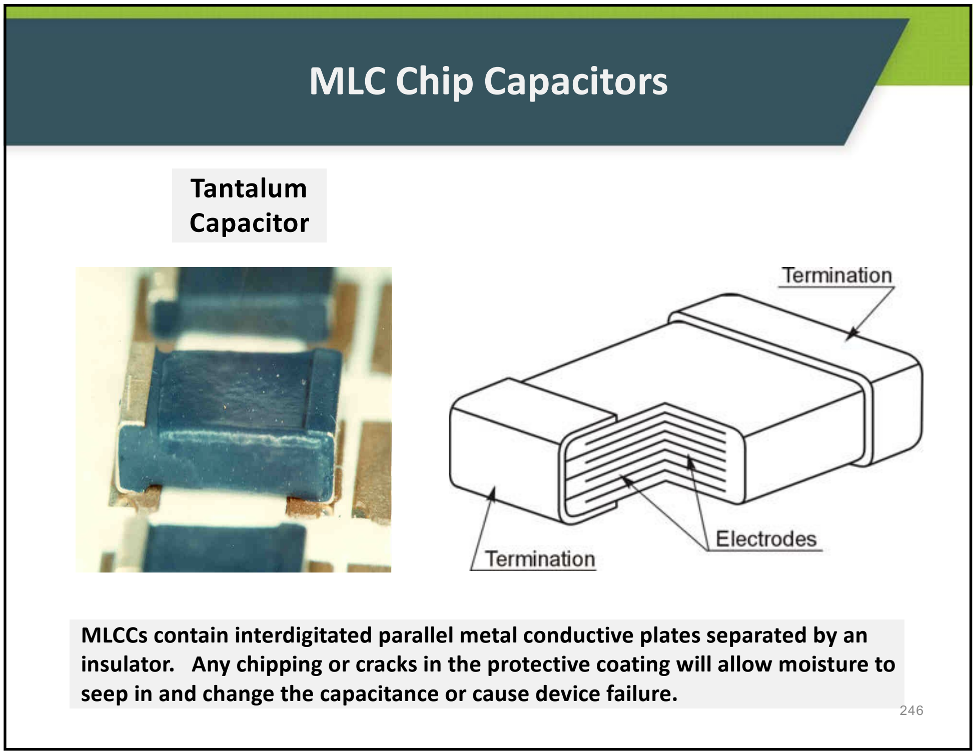
Course Notes



Lifted Trace on Duroid Substrate

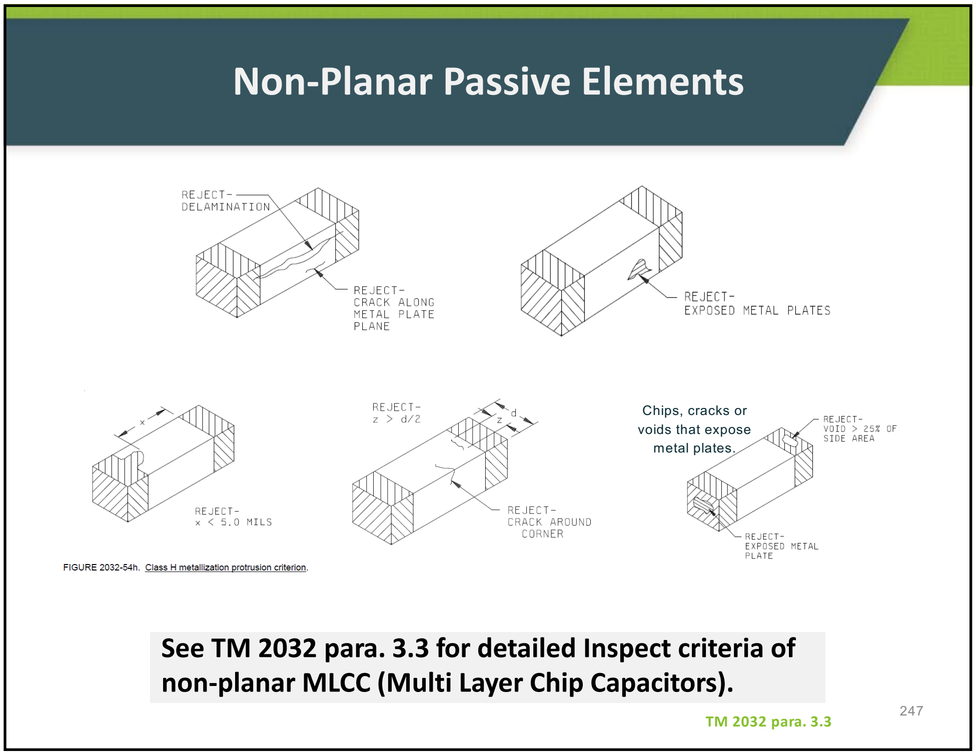
REJECT

Reject ..Lifted metal runs on teflon substrate caused by handling damage. (12X)



MLC Chip Capacitors

MLCCs contain interdigitated parallel metal conductive plates separated by an insulator. Any chipping or cracks in the protective coating will allow moisture to seep in and change the capacitance or cause device failure.



Non-Planar Passive Elements

Chips, cracks or voids that expose metal plates.

FIGURE 2032-54h. Class H metallization protrusion criterion.

See TM 2032 para. 3.3 for detailed Inspect criteria of non-planar MLCC (Multi Layer Chip Capacitors).

TM 2032 para. 3.3

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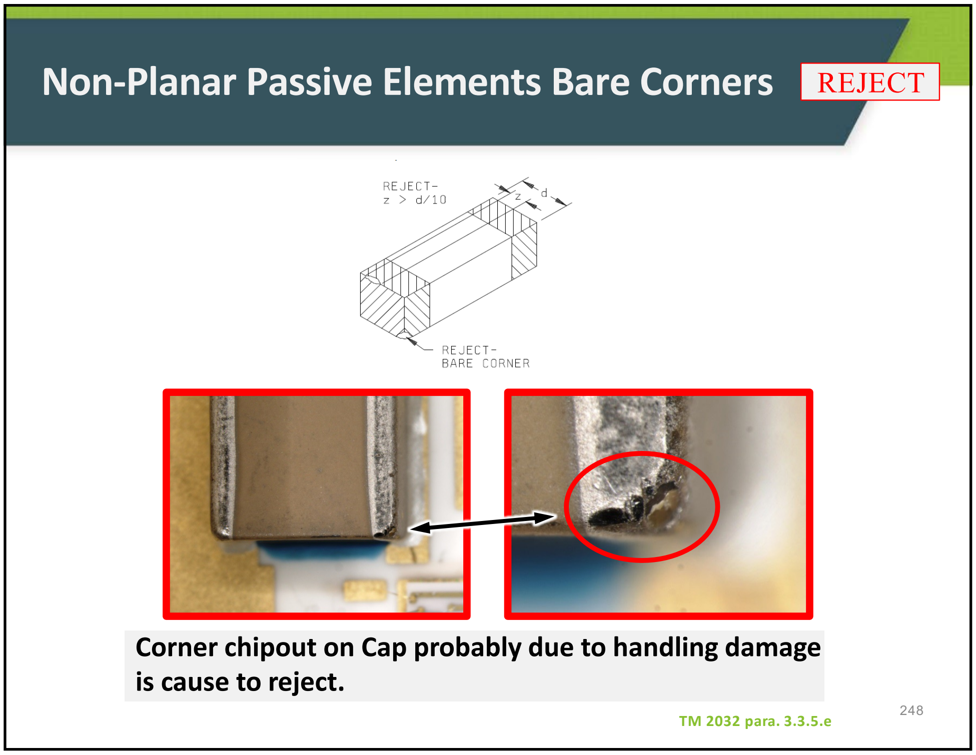


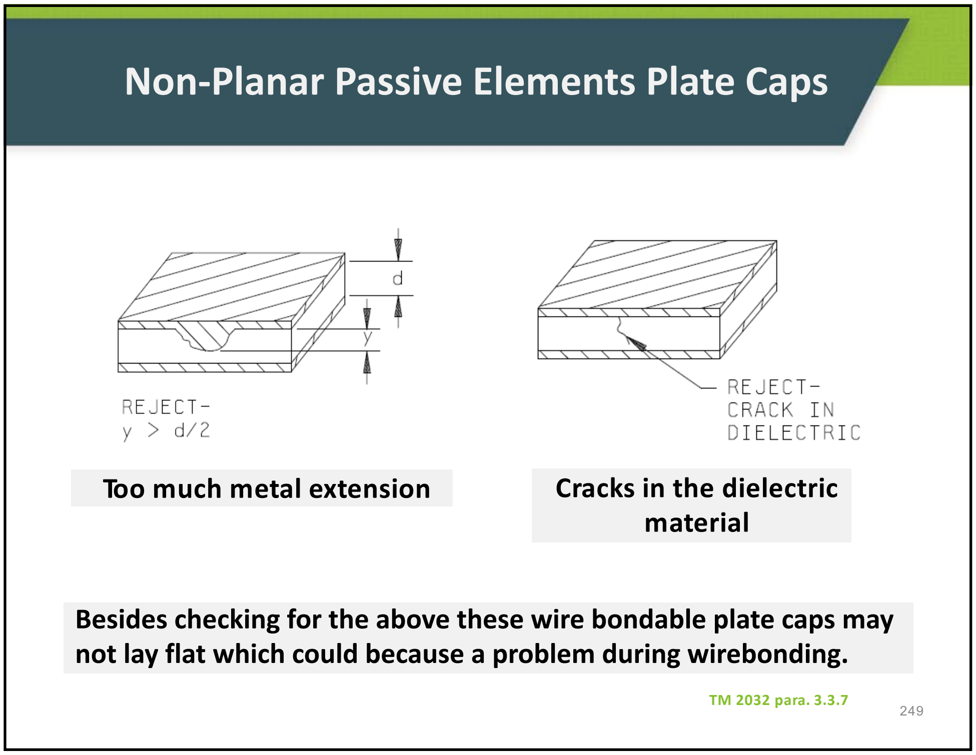
Non-Planar Passive Elements Bare Corners

REJECT

Corner chipout on Cap probably due to handling damage is cause to reject.

TM 2032 para. 3.3.5.e

248



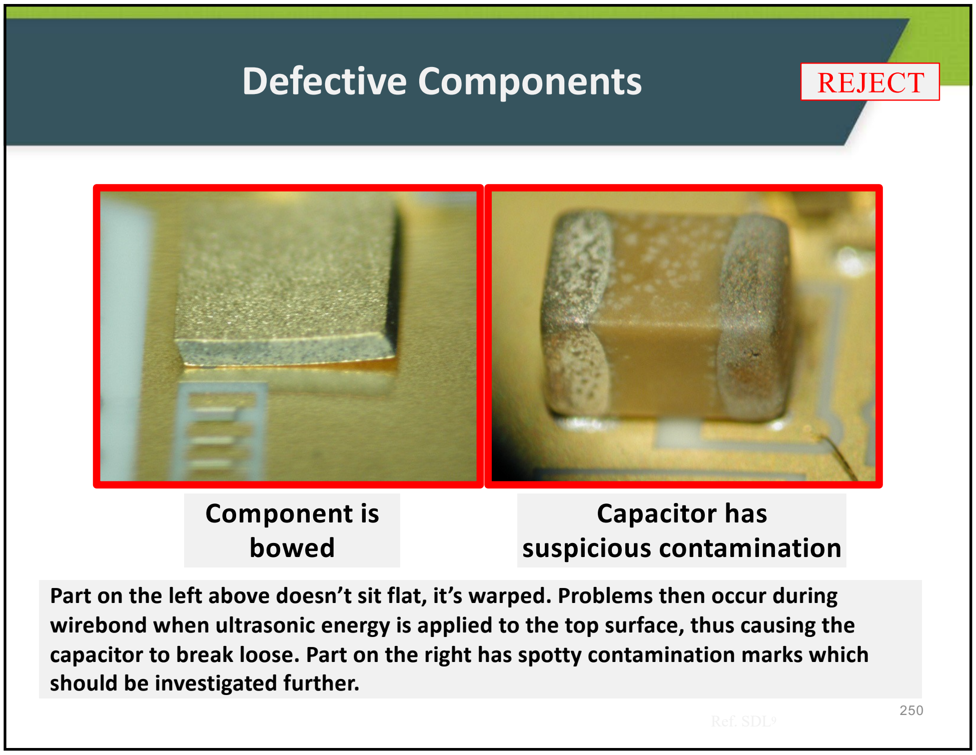
Non-Planar Passive Elements Plate Caps

Too much metal extension

Cracks in the dielectric material

Besides checking for the above these wire bondable plate caps may not lay flat which could because a problem during wirebonding.

TM 2032 para. 3.3.7



Defective Components

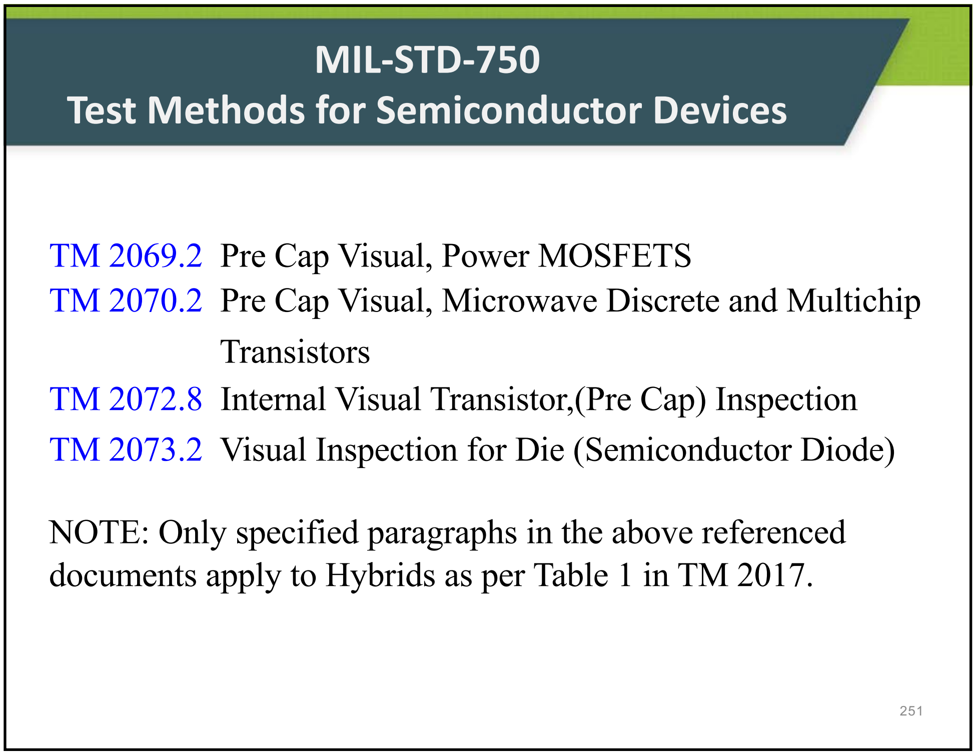
REJECT

Component is bowed

Capacitor has suspicious contamination

Part on the left above doesn't sit flat, it's warped. Problems then occur during wirebond when ultrasonic energy is applied to the top surface, thus causing the capacitor to break loose. Part on the right has spotty contamination marks which should be investigated further.

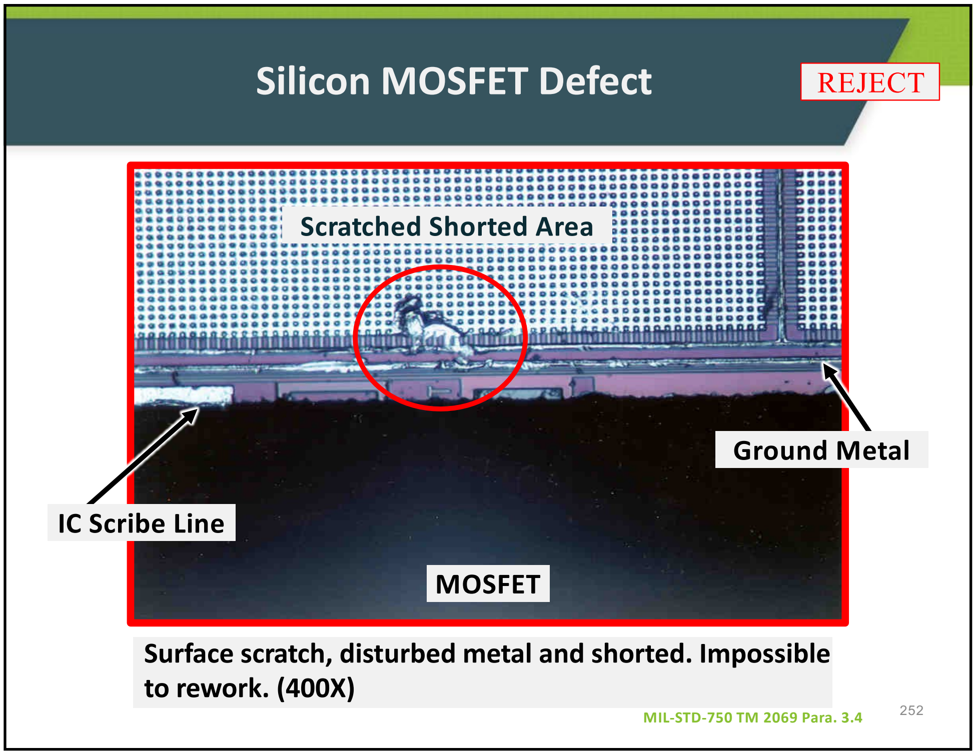
Ref. SDL



MIL-STD-750
Test Methods for Semiconductor Devices

TM 2069.2	Pre Cap Visual, Power MOSFETS
TM 2070.2	Pre Cap Visual, Microwave Discrete and Multichip Transistors
TM 2072.8	Internal Visual Transistor,(Pre Cap) Inspection
TM 2073.2	Visual Inspection for Die (Semiconductor Diode)

NOTE: Only specified paragraphs in the above referenced documents apply to Hybrids as per Table 1 in TM 2017.

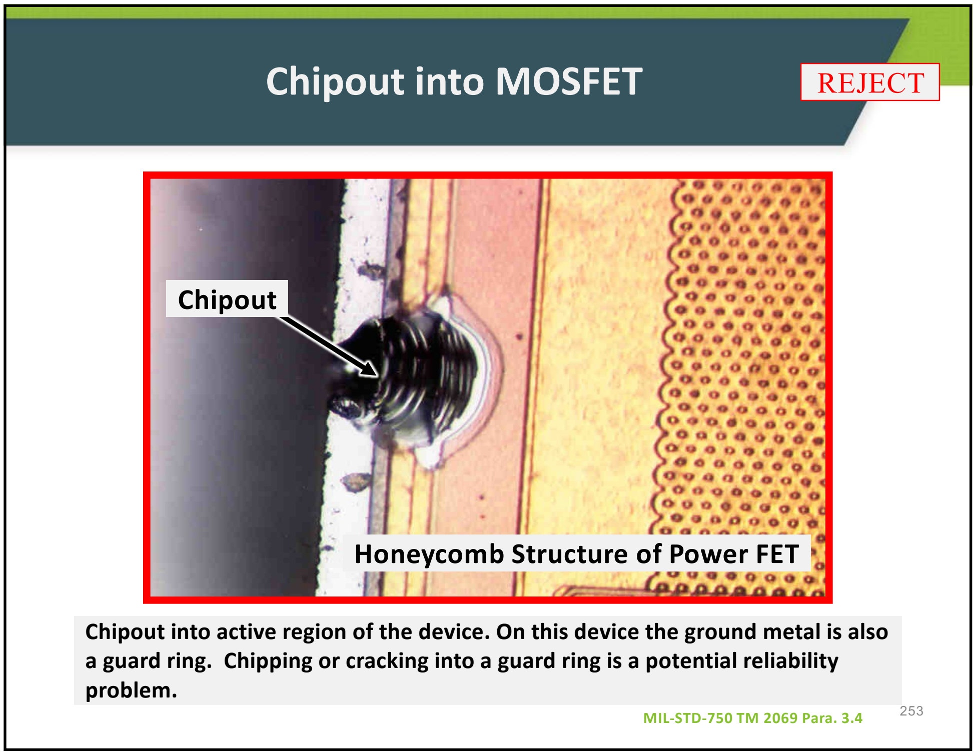


Silicon MOSFET Defect

REJECT

Surface scratch, disturbed metal and shorted. Impossible to rework. (400X)

MIL-STD-750 TM 2069 Para. 3.4

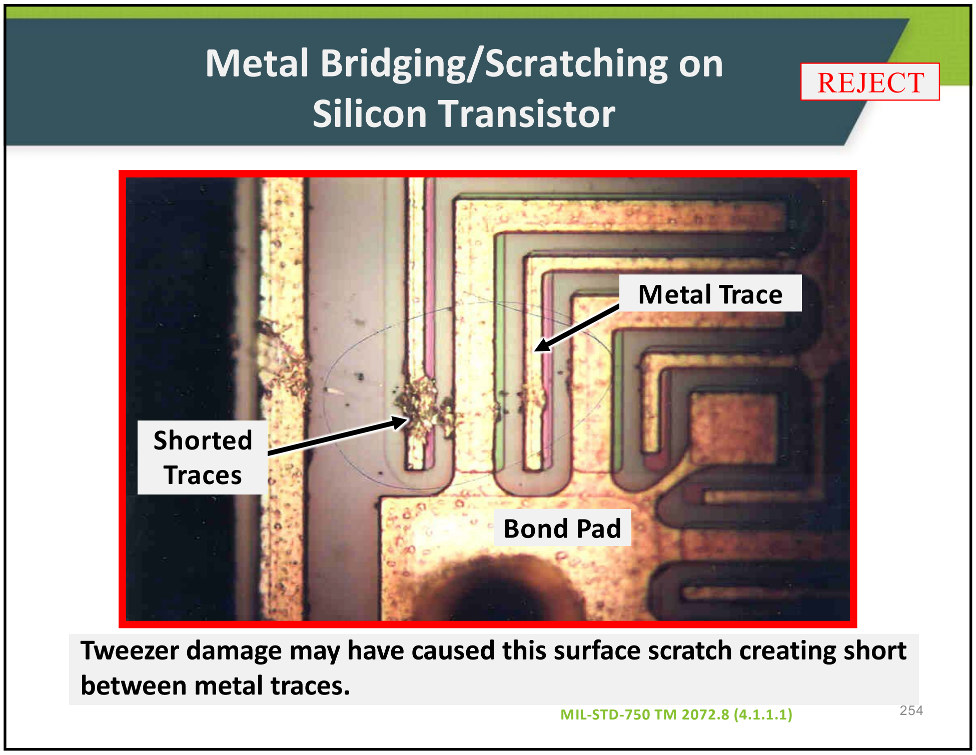


Chipout into MOSFET

REJECT

Chipout into active region of the device. On this device the ground metal is also a guard ring. Chipping or cracking into a guard ring is a potential reliability problem.

MIL-STD-750 TM 2069 Para. 3.4



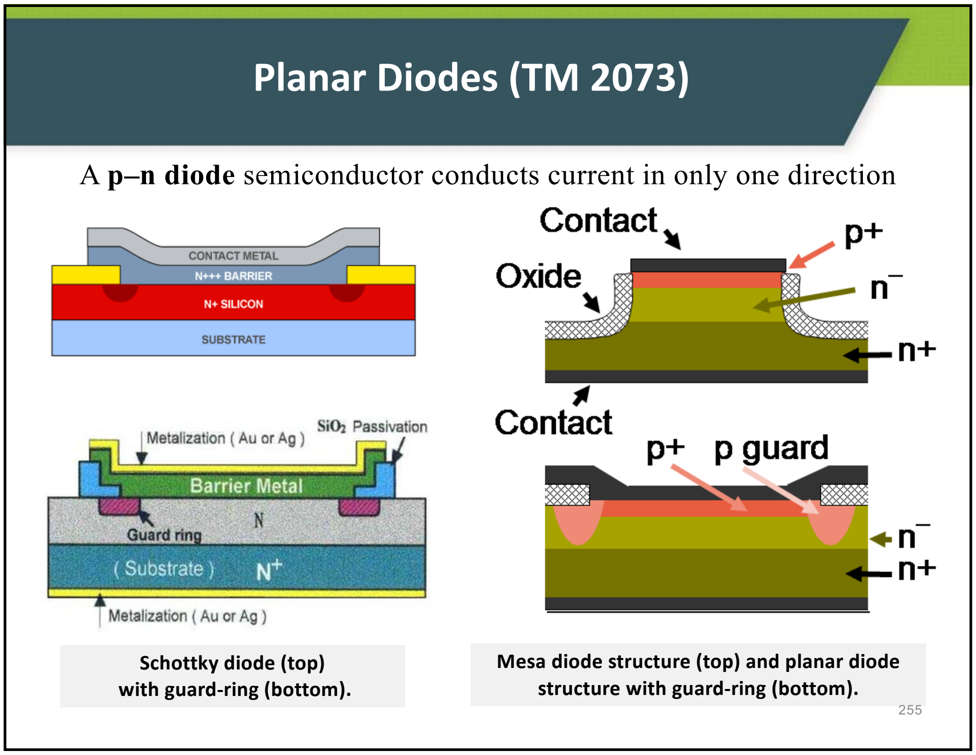
Metal Bridging/Scratching on Silicon Transistor

REJECT

Tweezer damage may have caused this surface scratch creating short between metal traces.

MIL-STD-750 TM 2072.8 (4.1.1.1)

Course Notes

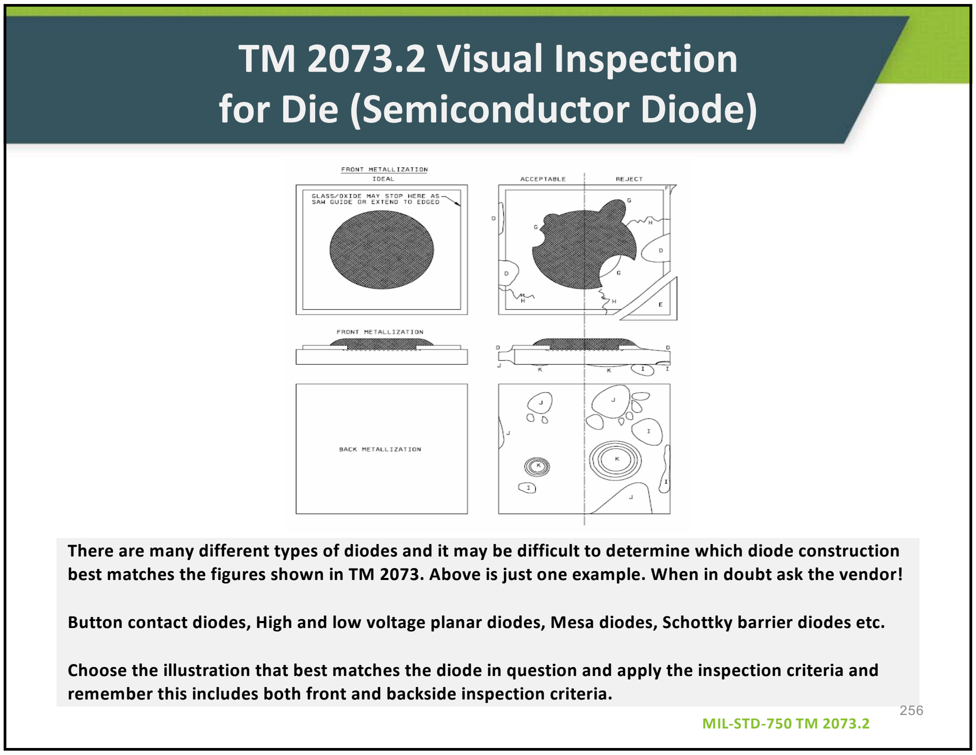


Planar Diodes (TM 2073)

A **p–n diode** semiconductor conducts current in only one direction

Schottky diode (top) with guard-ring (bottom).

Mesa diode structure (top) and planar diode structure with guard-ring (bottom).



TM 2073.2 Visual Inspection for Die (Semiconductor Diode)

There are many different types of diodes and it may be difficult to determine which diode construction best matches the figures shown in TM 2073. Above is just one example. When in doubt ask the vendor!

Button contact diodes, High and low voltage planar diodes, Mesa diodes, Schottky barrier diodes etc.

Choose the illustration that best matches the diode in question and apply the inspection criteria and remember this includes both front and backside inspection criteria.

MIL-STD-750 TM 2073.2

Course Notes

Chipouts without Guard Rings

MARGINAL

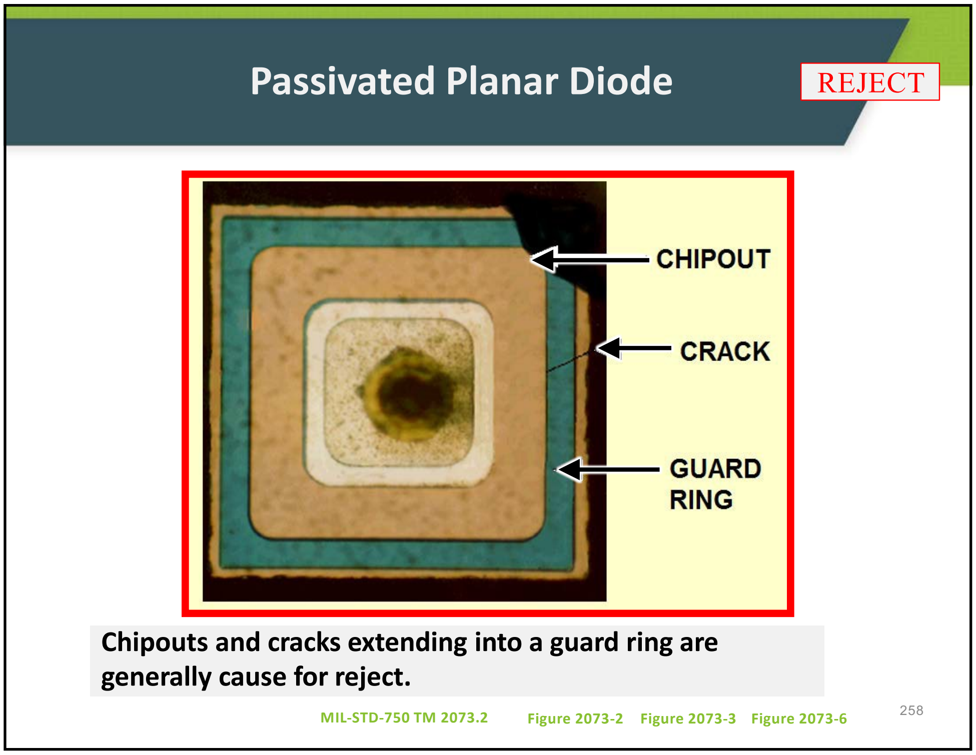
REJECT

Marginal chipout not into contact metal

Chipout into contact metal

MIL-STD-750 TM 2070 (3.4)

MIL-STD-750 TM 2072 (4.1.3)



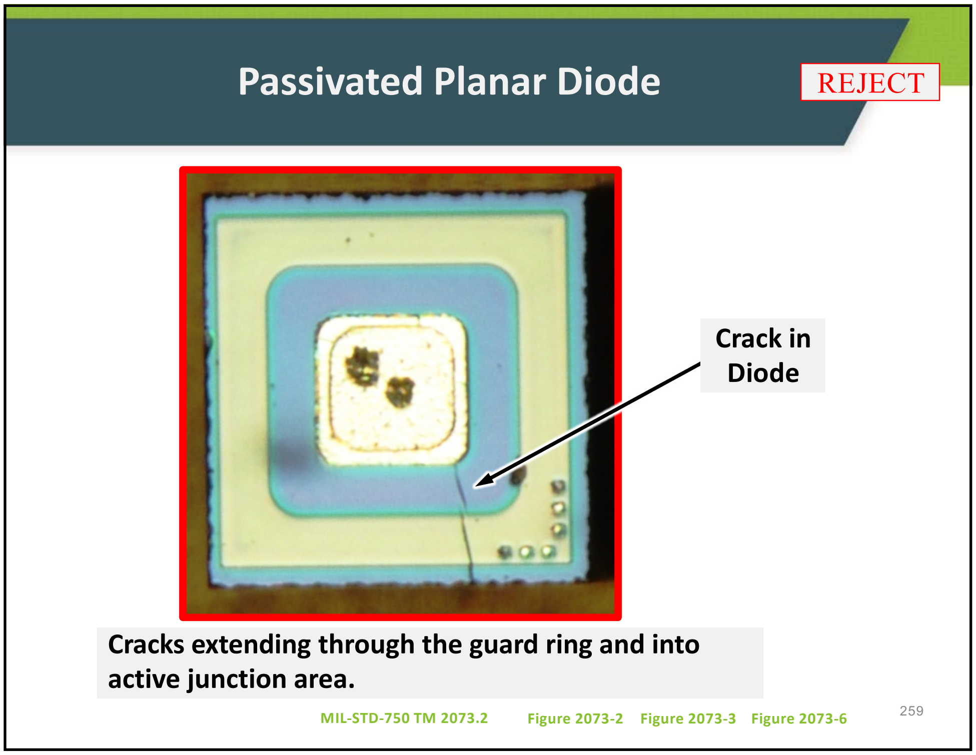
Passivated Planar Diode

REJECT

Chipouts and cracks extending into a guard ring are generally cause for reject.

MIL-STD-750 TM 2073.2 Figure 2073-2 Figure 2073-3 Figure 2073-6

Course Notes



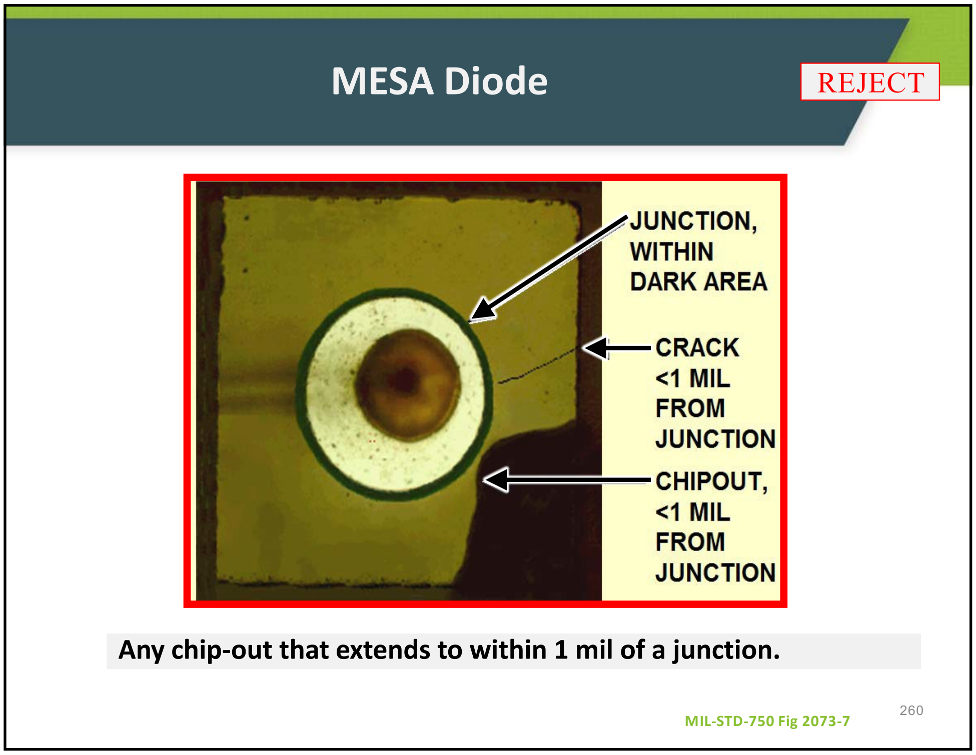
Passivated Planar Diode

REJECT

Crack in Diode

Cracks extending through the guard ring and into active junction area.

MIL-STD-750 TM 2073.2 Figure 2073-2 Figure 2073-3 Figure 2073-6



MESA Diode

REJECT

JUNCTION, WITHIN DARK AREA

CRACK <1 MIL FROM JUNCTION

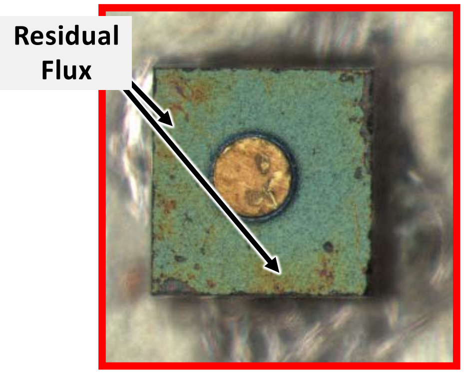
CHIPOUT, <1 MIL FROM JUNCTION

Any chip-out that extends to within 1 mil of a junction.

MIL-STD-750 Fig 2073-7

Varactor Diode MESA Structure

REJECT



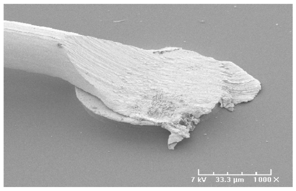
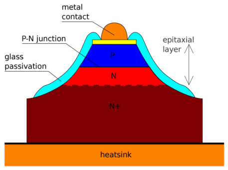


Figure 1.g: SEM image of wedge bond at die, 1000X

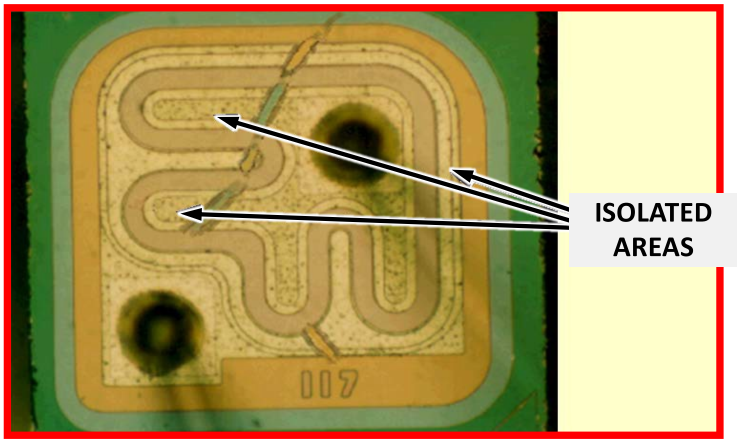


Brownish stains on surface is flux residue from solder attach. Flux is an organic acid and when combined with water can lead to corrosion and interfere with wirebonding. A varactor diode is a P-N junction diode that changes its capacitance and series resistance as the bias applied to the diode is varied.

Figure 2073-7

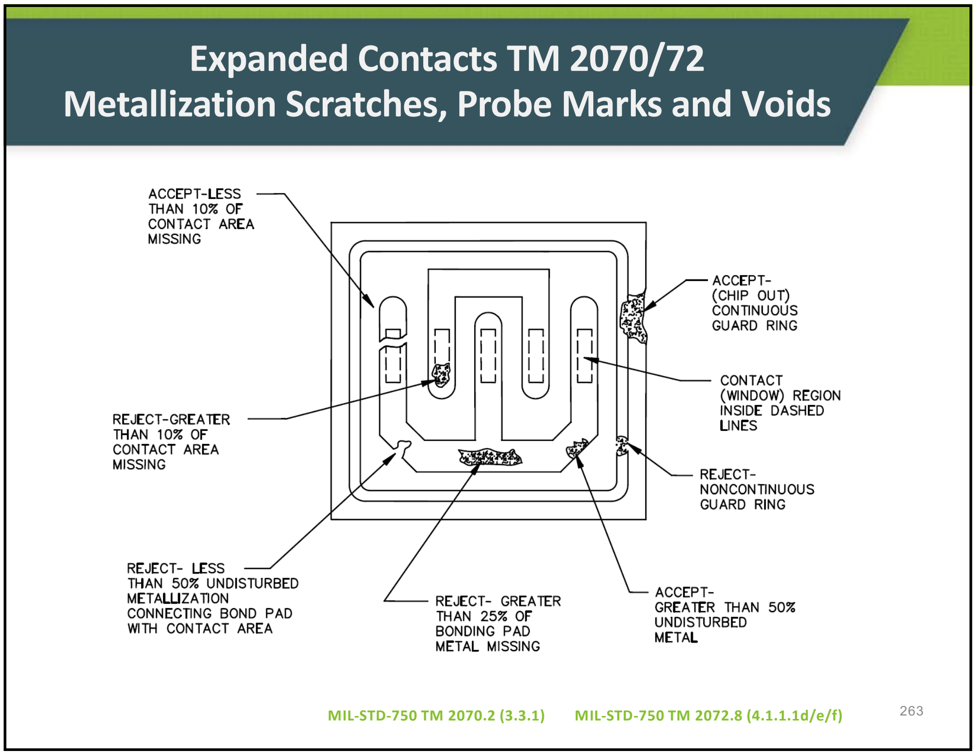
Scratch in Contact Region Non-Expanded Contacts

REJECT



Any scratch, probe mark or void, whether or not underlying material is exposed, which isolates more than 25 percent of the total metallization of an active region from the bonding pad.

MIL-STD-750 TM 2072.8 (4.1.1.1c)



Expanded Contacts TM 2070/72 Metallization Scratches, Probe Marks and Voids

ACCEPT-LESS THAN 10% OF CONTACT AREA MISSING

ACCEPT- (CHIP OUT) CONTINUOUS GUARD RING

CONTACT (WINDOW) REGION INSIDE DASHED LINES

REJECT-GREATER THAN 10% OF CONTACT AREA MISSING

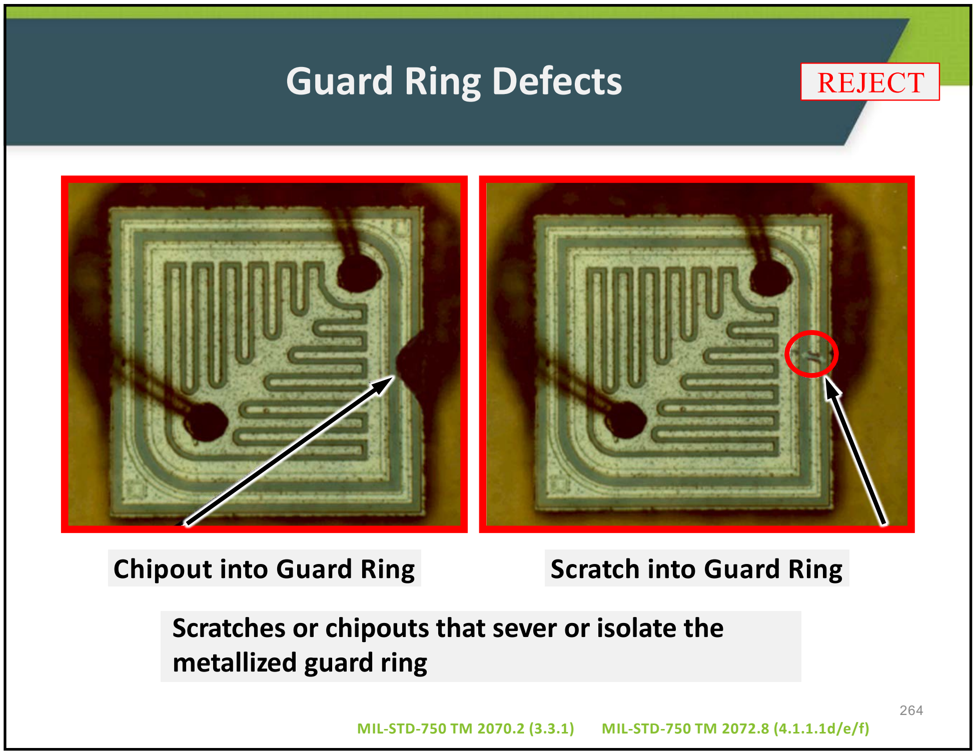
REJECT- NONCONTINUOUS GUARD RING

REJECT- LESS THAN 50% UNDISTURBED METALLIZATION CONNECTING BOND PAD WITH CONTACT AREA

REJECT- GREATER THAN 25% OF BONDING PAD METAL MISSING

ACCEPT- GREATER THAN 50% UNDISTURBED METAL

MIL-STD-750 TM 2070.2 (3.3.1) MIL-STD-750 TM 2072.8 (4.1.1.1d/e/f)



Guard Ring Defects

REJECT

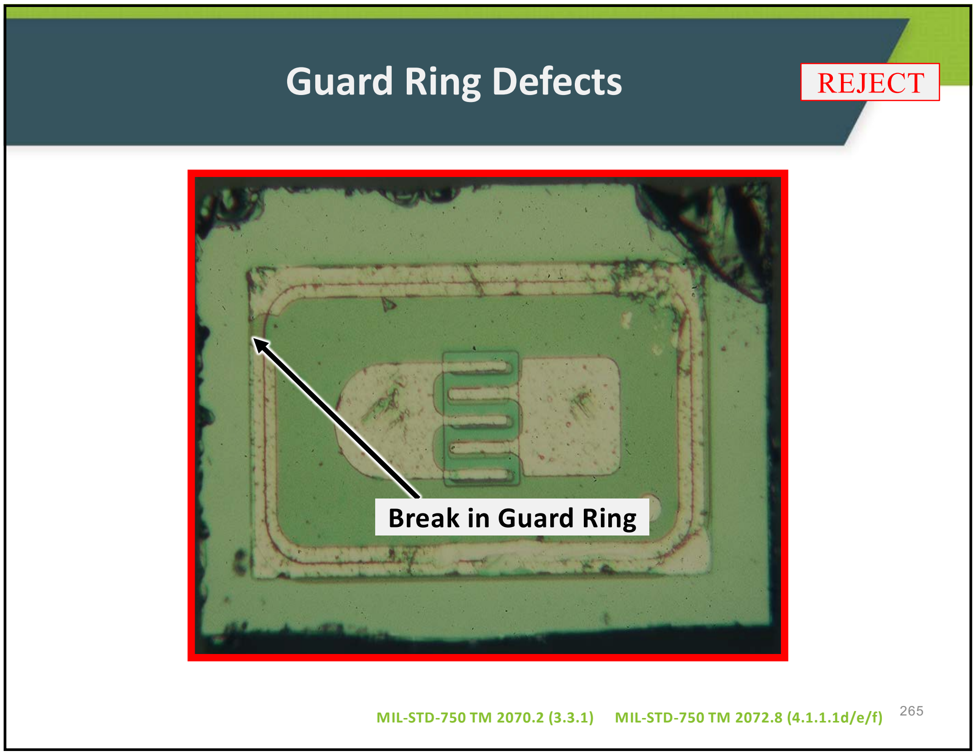
Chipout into Guard Ring

Scratch into Guard Ring

Scratches or chipouts that sever or isolate the metallized guard ring

MIL-STD-750 TM 2070.2 (3.3.1) MIL-STD-750 TM 2072.8 (4.1.1.1d/e/f)

Course Notes

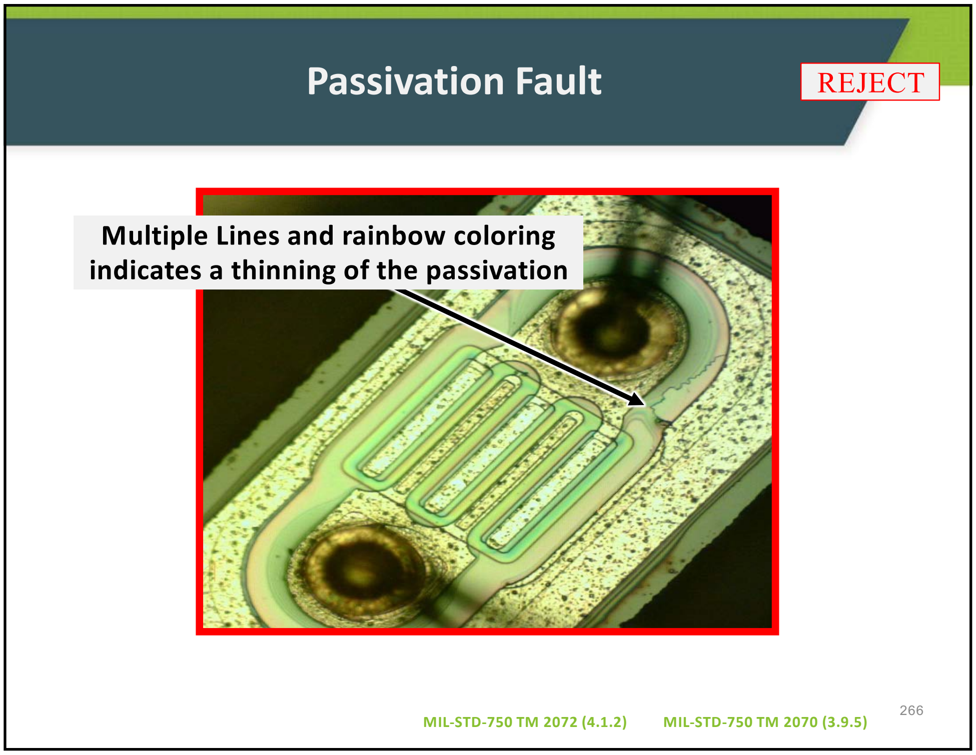


Guard Ring Defects

REJECT

Break in Guard Ring

MIL-STD-750 TM 2070.2 (3.3.1) MIL-STD-750 TM 2072.8 (4.1.1.1d/e/f)

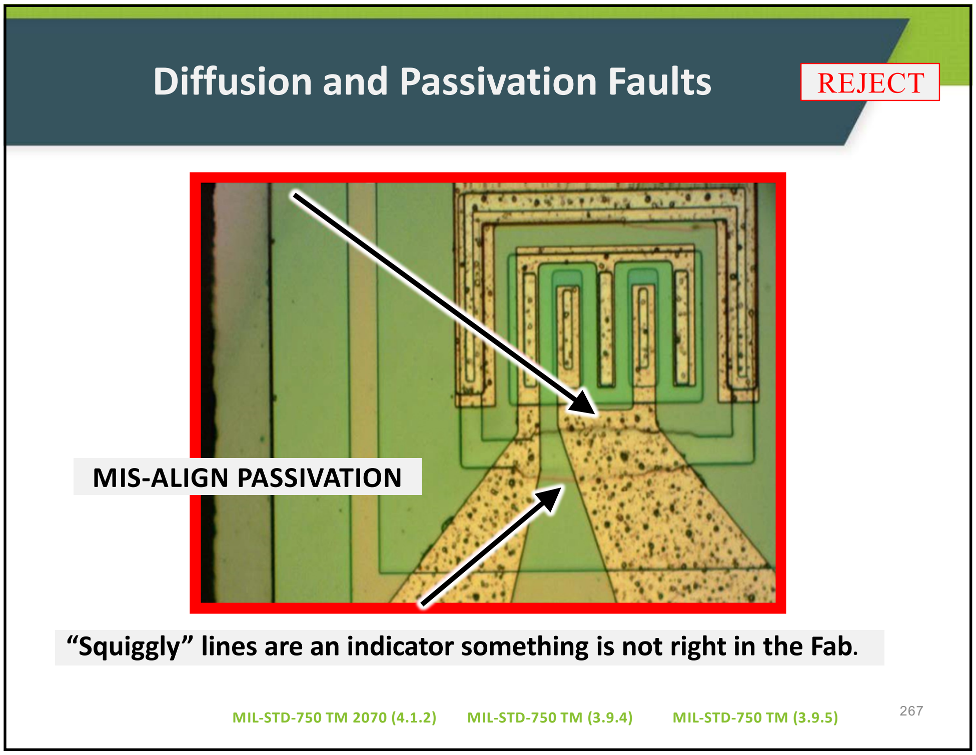


Passivation Fault

REJECT

Multiple Lines and rainbow coloring indicates a thinning of the passivation

MIL-STD-750 TM 2072 (4.1.2) MIL-STD-750 TM 2070 (3.9.5)

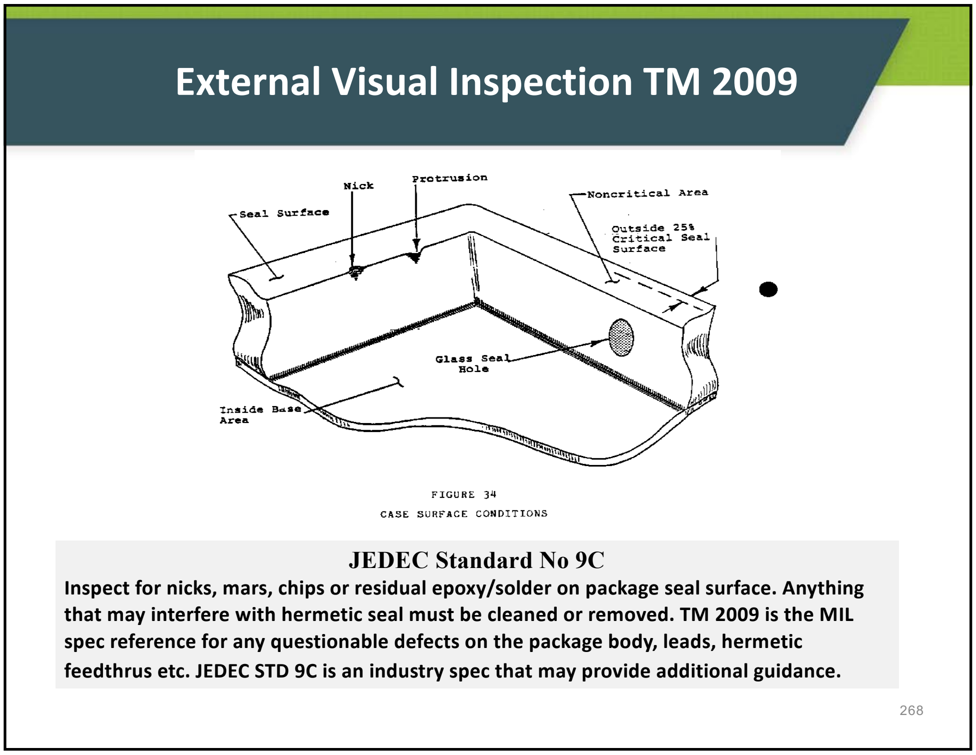


Diffusion and Passivation Faults

REJECT

"Squiggly" lines are an indicator something is not right in the Fab.

MIL-STD-750 TM 2070 (4.1.2) MIL-STD-750 TM (3.9.4) MIL-STD-750 TM (3.9.5)



External Visual Inspection TM 2009

FIGURE 34
CASE SURFACE CONDITIONS

JEDEC Standard No 9C

Inspect for nicks, mars, chips or residual epoxy/solder on package seal surface. Anything that may interfere with hermetic seal must be cleaned or removed. TM 2009 is the MIL spec reference for any questionable defects on the package body, leads, hermetic feedthrus etc. JEDEC STD 9C is an industry spec that may provide additional guidance.

Metal Burrs on the Package

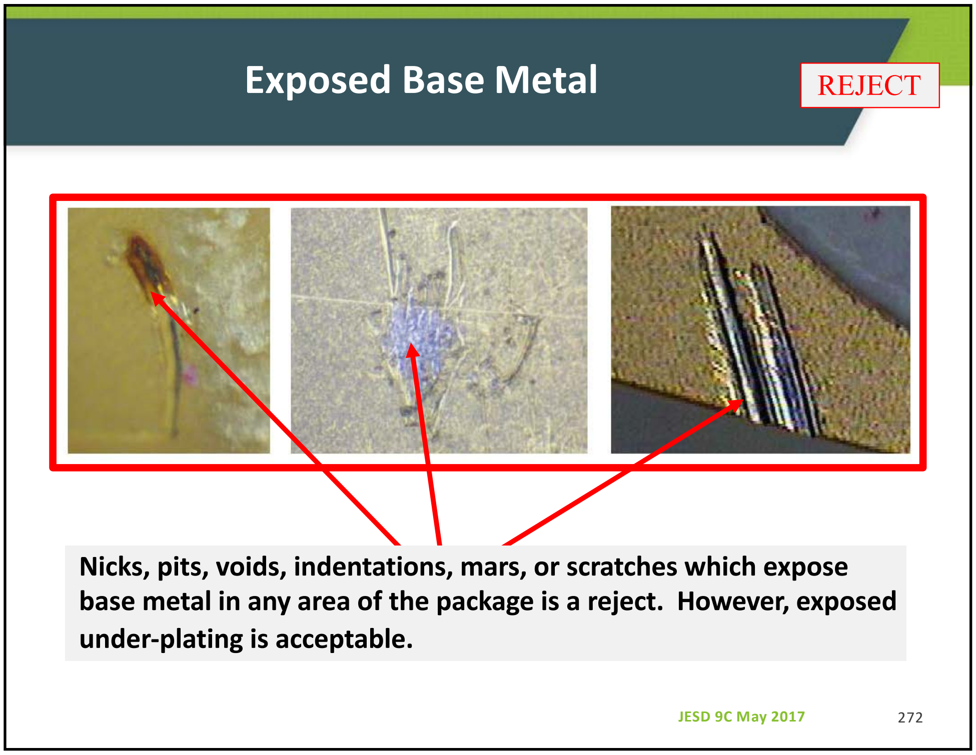
REJECT

Exposed base metal

Metal Burrs

Metal burrs inside or outside of the hermetic enclosure can break off can cause a short. Any burr that prevents the package from laying flat is often a problem. Exposed base metal . . . usually nickel or Kovar can corrode.

TM 2009 Para. 3.3.4



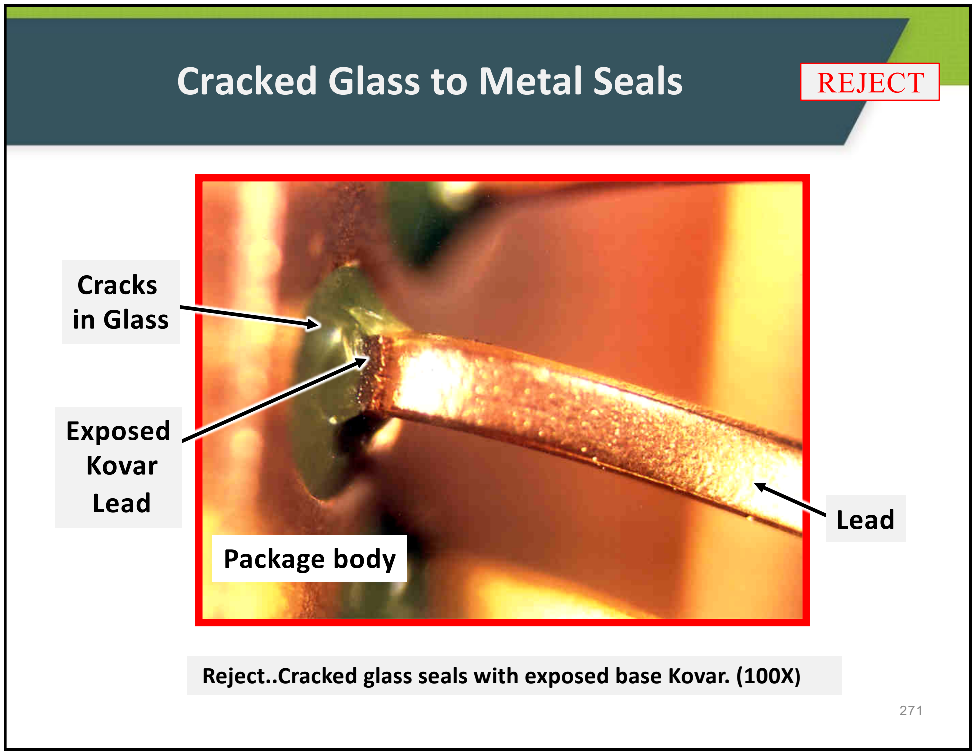
Exposed Base Metal

REJECT

Nicks, pits, voids, indentations, mars, or scratches which expose base metal in any area of the package is a reject. However, exposed under-plating is acceptable.

JESD 9C May 2017

Course Notes



Cracked Glass to Metal Seals

REJECT

Cracks in Glass

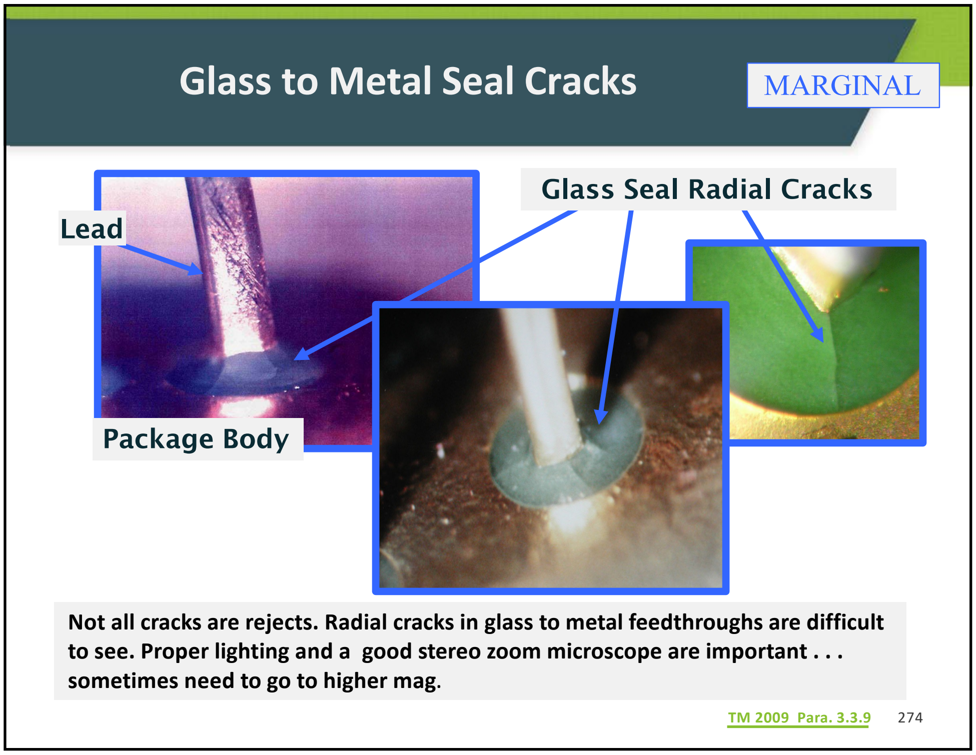
Exposed Kovar Lead

Lead

Package body

Reject..Cracked glass seals with exposed base Kovar. (100X)

271



Glass to Metal Seal Cracks

MARGINAL

Glass Seal Radial Cracks

Lead

Package Body

Not all cracks are rejects. Radial cracks in glass to metal feedthroughs are difficult to see. Proper lighting and a good stereo zoom microscope are important . . . sometimes need to go to higher mag.

TM 2009 Para. 3.3.9

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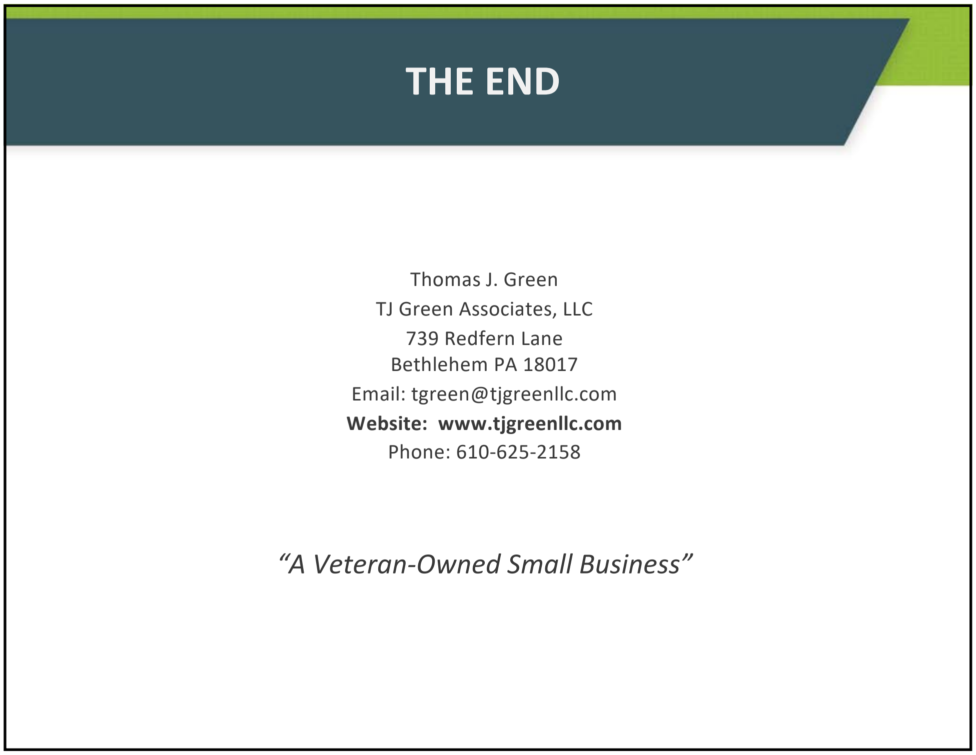

THE END

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